Florida 2070 Advanced Traffic Controller Minimum Specifications

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__ State Traffic Engineering Office__
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SECTION 1 - GENERAL

1.1 Unit Configuration

This specification is to address Model 2070 Advanced Traffic Controller (2070 UNIT) for the certification and use in the state of Florida. The 2070 UNIT is the fully expanded configuration with full VME capability. The minimum specified configuration (2070 LITE) shall be downward compatible to operate in a 170 cabinet as a single intersection controller assembly. This specification is derived from the publication "*Advanced Transportation Controller (ATC) Standard Specification for the Type 2070 Controller*" by AASHTO/ITE/NEMA.

1.1.1 The 2070 Unit Controller shall be composed of the following components:

UNIT CHASSIS
MODEL 2070-1A CPU MODULE, MULTIPLE BOARD-VME
MODEL 2070-2A FIELD I/O MODULE (FI/O for 170 Cab)
MODEL 2070-3 FRONT PANEL MODULE (FP), Option A, B or C (Blank)
MODEL 2070-4A POWER SUPPLY MODULE, 10 AMP
MODEL 2070-5 VME CAGE ASSEMBLY

1.1.2 The communications and option modules/assemblies shall be called out separately from the 2070 Controller unit. The composition weight shall not exceed 11.3 kilograms.

1.2 Metalwork

The Chassis Enclosure, Internal Structure Supports, Back Plane Mounting Surface, Module Plates, Cover Plates, Power Supply Enclosure, and Front Panel shall be made of 1.524 mm minimum Aluminum Sheet.

1.3 Power Limitations

Controller Module/Assembly power limitations shall be as follows:

Model/Component	+5VDC	+12VDC iso	+12VDC ser	-12 VDC ser
MCB	750 mA	-----	-----	-----
TRANS BD	750 mA	-----	-----	-----
2070-2A FI/O	250 mA	750 mA	-----	-----
2070-3A FPA	500 mA	-----	-----	-----
2070-5 VME	5.0 A	-----	200 mA	200 mA
2070-6 All Comm	500 mA	-----	100 mA	100 mA
2070-7 All Comm	250 mA	-----	50 mA	50 mA

1.4 EIA-485 Communications Circuitry

All circuitry associated with the EIA-485 Communications links shall be capable of reliably passing a minimum of 1.0 megabits per second. Isolation circuitry shall be by opto- or capacitive-coupled isolation technologies.

1.5 EIA-485 Line Drivers/Receivers

The EIA-485 Line Drivers/Receivers shall be socket mounted and shall not draw more than 35 mA in active state and 20 mA in inactive state. A 100-Ohm Termination Resistor shall be provided across each Differential Line Receiver Input. The MOTHERBOARD's control signals (e.g., SP1-RTS) shall be active, or asserted, when the positive terminal (e.g., SP1-RTS+) is a lower voltage than its corresponding negative terminal (e.g., SP1-RTS-). A control signal is inactive when its positive terminal voltage is higher than its negative terminal. Receive and transmit data signals shall be read as a "1" when the positive terminal's (e.g., SP1-TXD+) voltage is higher than its corresponding negative terminal (e.g., SP1-TXD-). A data value is "0" when its positive terminal's (e.g., SP1-TXD+) voltage is lower than its negative terminal (e.g., SP1-TXD-).

1.6 MTBF Analysis Report

A Mean-Time-Between-Failure Analysis Report shall be provided with the Qualified Products List Submittal. It shall encompass the 2070 Controller (the complete system) and its individual modules/assemblies. The report shall describe in detail the methodology used.

1.7 Sockets

Sockets for devices (called out to be socket mounted) shall be "xx" pin AUGAT 500/800 series AG10DPC or equal.

1.8 SDLC

SP5and SP3 SDLC frame address assignments (Command/Response) are as follows:

		SP5	*SP3*
CPU 2070-1	=	“19”	“19”
FI/O 2070-2A	=	“20”	Not Applicable
CPU Broadcast to all	=	“127”	“255”

All other addresses are reserved by the AGENCY. The SDLC response frame address shall be the same address as the Command frame it receives.

1.9 Year 2000 Compliance

The 2070 UNIT shall comply with the State Year 2000 Compliance:
"Year 2000 compliance for Systems in the State of Florida is achieved when an application or system products (including software, microcode and microprocessors), programs, files, databases, and functionality have or create no logical or mathematical inconsistencies when dealing with dates prior to and beyond 1999. The year 2000 is recognized and processed as a leap year. The product must also operate accurately in the manner in which it was intended for date operation without requiring manual intervention."

1.10 Florida Requirements

1.10.1 Backward Compatibility

Controller internal coordinator shall be interoperable with the same manufacturer's Controller internal coordinator of earlier models.

1.10.2 Start-Up Sequence

Upon restoration of power, a vehicle call (as a minimum) shall be placed on all phases. The start-up sequence shall be programmable to start at the beginning of the green or yellow interval of any selected phase or non-conflicting phase pair. Unless otherwise stipulated in the contract documents the start-up sequence shall begin with the major street (movements 2 and 6) green interval and serve in preferential sequence, all phases with at least a minimum recall or the summation of pedestrian walk and clearance interval. The start-up sequence shall end with the major street left turn green interval (movements 1 and 5), at which time the controller unit shall operate as an actuated controller.

1.10.3 Timing

1.10.3.1 Accuracy of Intervals:

Settability: The settability shall be fixed discrete increments.
Repeatability: The digital timing shall relate to the input line frequency such that no cumulative or drift errors will occur in timing intervals. No interval shall deviate by more than plus or minus 100 ms from its set value, at a power source frequency of 60 Hz.

1.10.3.2 Interval Timing:

The following intervals, with the associated timing ranges and maximum increments, shall be provided for each phase of the controller unit:

Minimum Interval	Range (Seconds)	Maximum Increment (Seconds)
Minimum Green	1-30	1.0
Passage Time	*0-9	0.1
Maximum Green I & II	1-99	1.0
Yellow Clearance	3-7	0.1
Red Clearance	*0-7	0.1
Walk	1-30	1.0
Pedestrian Clearance	*0-30	1.0

*Zero shall be satisfied by any time between zero and 100 ms.
Yellow clearance shall not be less than three seconds.

When volume density features are specified in the contract documents, the following intervals with the associated timing ranges and maximum increments shall be provided for each phase of the controller unit:

Interval	Minimum Range (Seconds)	Maximum Increment (Seconds)
Added initial	*0-3 per actuation	0.1
Time to reduce	1-60	1.0
Time before reduction	1-60	1.0
Minimum gap	0-7.75	0.1

*Zero shall be satisfied by any time between zero and 100 ms.

1.10.4 Preemption Operation
The logic for controlling railroad, bridge and fire preemption signal sequences and timing shall be contained internally in the controller unit.
When the controller unit is in the non-preemption green movement and the preemption circuit is activated, a minimum green time from three to 30 seconds (adjustable in 1 second increments) shall be timed by the preemption logic. If a pedestrian walk interval is timing upon activation of the preemption circuit, the preemption logic shall immediately advance the controller unit to the pedestrian clearance interval. The setting of the minimum green time shall be the pedestrian clearance interval time. The timing ranges for all other preemption intervals shall be as shown in the plans.

An additional Connector shall be furnished for the preemption interconnect signal. This additional connector can be Connector D as specified in 671-20 and shall not interface with the controller's standard I/O connector(s).

1.10.5 Coordination Units
Traffic signal system coordination whose function is to control the timed relationship between intersections so as to maintain a system interconnect plan are covered below. Coordination functions to control intersection cycle lengths, system offsets, and phase splits shall be provided as a standard feature, with no need for additional modules or software.

1.10.6 Cycle Split Sets
A cycle split set is defined as a percentage of the cycle length allocated to the various phases of the controller unit.

1.10.6.1 Timing Requirements: The timing controls for programming the cycle length, offsets, force-off points and permissive periods shall be as approved by the Department. All timing controls shall be color or function coded.

The timing of all functions shall be digital and use the 60 Hz power as the reference. The timing accuracy of any interval shall not deviate by more than ±100 ms from its set value at a power source frequency of 60 Hz.

The timing ranges and maximum increments of adjustment for the various timing functions of coordination units shall be as indicated in the chart below:

Function	Minimum Timing Range	Maximum Increment of Adjustment
Cycle Length	40 to 255 seconds	1 second
Offsets	0 to 255 seconds or 1 to 99 percent of cycle length	1 second or 1 percent of cycle length
Force-off points		
Permissive Periods		

1.10.7 Clock Circuit for TBC

The clock circuit of the TBC units may use either the 60 Hz AC power source or a crystal oscillator as the timing reference. If a crystal oscillator is used as the timing reference, the frequency tolerance of the clock circuit shall be ±0.0015%. The clock circuit of the TBC unit shall be settable to the nearest second.

The TBC unit shall be provided with a programmable feature which automatically changes from standard time to daylight savings time and vice versa.

1.10.8 Battery Power

The TBC units shall be provided with a battery to power the clock circuit and memory for a minimum of 6 months when the 120 V AC power source is disconnected, after batteries are fully charged.

The frequency tolerance of the clock circuit, when operated on battery power shall be ± 0.0015%. Repetitive transfer from battery power to 120 V AC power to battery power, and voltage brown-outs (voltage less than 96 V AC) shall not affect the accuracy of the TBC clock circuit.

SECTION 2 - TYPE 2070-1 CPU MODULE

2.1 Configuration

The 2070-1A CPU MODULE shall consist of the Main Controller Board (MCB), Transition Board, Board Interface Harness, and CPU Module Software.

2.2 Main Controller Board

2.2.1 General

The MCB shall be a 3U VME bus compliant board and contain a system controller, an A24-D16 interface, a Master & Slave bus interface, a Multilevel VMEbus Arbiter, a FAIR VMEbus Requester and BTO(64).

2.2.2 Controller

The CONTROLLER Device shall be a Motorola MC68360 or better, clocked at 24.576 MHz minimum. The Interrupts shall be configured as follows:

Level 7 - VMEbus IRQ7, ACFAIL
Level 6 - VMEbus IRQ6, OS-9 Operating System TICK Timer
Level 5 - VMEbus IRQ5
Level 4 - VMEbus IRQ4, CPU Module Counters / Timers, LINESYNC (auto vectored), Serial Interface Interrupts
Level 3 - VMEbus IRQ3
Level 2 - VMEbus IRQ2
Level 1 - VMEbus IRQ1

2.2.2.1 The Fast IRQ Service System is reserved for State use only.

2.2.3 Memory Address Organization

8000 0000 - 80FF FFFF	STANDARD
9000 0000 - 9000 FFFF	SHORT

2.2.3.1 Sixteen (16) megabytes of contiguous address space for each specified memory (DRAM, SRAM and FLASH) shall be allocated on an even boundary. The SRAM and FLASH memories shall be accessed through the OS-9 Operating System's RBF Manager. The address of each memory block shall be specified by the Contractor and provided with the documentation.

2.2.3.2 When the incoming +5 VDC falls below its operating level, the SRAM shall shift to the +5 VDC Standby Power supply and drop to its standby state. The TOD Clock shall shift to its own standby power source. When the incoming +5 VDC rises to within its operating level, the appropriate MCB Circuitry shall shift from standby power to incoming +5 VDC.

2.2.4 RAM Memory

A minimum of 4 MB of DRAM, organized in 32-bit words, shall be provided. A minimum of 512 KB of SRAM, organized in 16- or 32-bit words, shall be provided. The SRAM shall draw no more than 50 μA at +5 VDC in Standby Mode. The time from the presentation of valid RAM address, select lines, and data lines to the RAM device to the acceptance of data by the RAM device shall not exceed 80 ns and shall be less than as required to fulfill zero-wait-state RAM device write-access under all operational conditions.

2.2.5 FLASH Memory

A minimum of 4 MB of FLASH Memory, organized in 16- or 32-bit words, shall be provided. The MCB shall be equipped with all necessary circuitry for writing to the FLASH Memory under program control. No more than 1 MB of FLASH Memory shall be used for Boot Image (List) and a minimum of 3 MB shall be available for STATE use.

2.2.6 Time-of-Day Clock

A software-controllable hardware Time-of-Day (TOD) Clock shall be provided. It shall, under standby power, operate for a minimum of 30 days maintaining an accuracy of ±1 minute per 30 days at 25° C. The clock shall maintain a minimum fractional second resolution of 10 ms and shall track fractional seconds, seconds, minutes, hours, day of month, month, and year.

2.2.7 CPU Reset

A software-driven CPU RESET signal (Active LOW) shall be provided to reset other controller systems. The signal output shall be driver capable of sinking 30 mA at 30 VDC. Execution of the program module “CPURESET” in the boot image shall assert the CPU RESET signal once.

2.2.8 CPU Activity Indicator

An open-collector output, capable of sinking 30 mA at 30 VDC, shall be provided to drive the Front Panel Assembly CPU Activity LED Indicator.

2.2.9 Tick Timer

The OS-9 Operating System TICK Timer shall be derived from the edge transition of LINESYNC with a tick rate of 120 ticks per second.

2.3 Transition Board

A Transition Board (TB) shall be provided to transfer serial communication and control signals between the MCB and the Interface Motherboard. Said signal and communication lines shall be driven/received off and on the module compliant to EIA- 485. The Transition Board shall provide a 1 K-Ohm pull-up resistor for the A2 & A3 installed lines. If the DC Ground is not present (slot not occupied) at the CPU EIA-485 line drivers/receivers, the drivers/receivers shall be disabled (inactive).

2.4 Shielded Interface Harness

A Shielded Interface Harness shall be provided. It shall include MCB and Transition Board connectors with strain relief, lock latch, mating connectors, and harness conductors. A minimum of 25 mm of slack shall be provided. No power shall be routed through the harness. The harness shall be 100% covered by an aluminum mylar foil and an extruded black 0.8 mm PVC jacket or equal.

2.5 Data Key

A DATAKEY Receptacle (KC4210, KC4210PCB or equal) with Key (DK1000or equal) resident shall be provided and mounted on the CPU module front panel (or the Transition Board of Type 1A). The Black DATAKEY shall be tested, interrogated and all 128 addresses read using Software Interface. Power shall not be applied to the receptacle if the key is not present.

2.6 CPU Module Software

The following software shall be supplied:

1. Operating System
2. Drivers and Descriptors
3. Application Kernel
4. Error Handler
5. Validation Suite
6. Deliverables

2.6.1 Operating System

The CPU Module shall be supplied with Microware Embedded OS-9 Version 3.03 software and, in addition, the following:

1. Embedded OS-9 Real Time Kernel
2. Sequential Character File Manager (SCFMAN)
3. Sequential Protocol File Manager (SPFMAN)
4. Pipe File Manager (PIPEMAN)
5. Random Block File Manager (RBFMAN)
6. C Input Output Library (CIO)

Boot Image shall include the following utility modules:

Break	Date	Deiniz	Devs	Free	Copy
Dir	Tmode	Edt	List	Load	Deldir
Dump	Del	Ident	Iniz	Irqs	Events
Echo	Kill	Dcheck	Cio	Link	Kermit
Lmm	Mdir	Mfree	Pd	Makdir	Save
Attr	Rename	Procs	Unlink	Sleep	Xmode
Shell	Build	Setime			

2.6.2 Drivers and Descriptors

2.6.2.1 Supplied modules shall be re-entrant, address independent, and shall not contain self-modifying code.

2.6.2.2 Drivers shall be provided to access the FLASH, SRAM, and DRAM memories through RBFMAN. The following RBFMAN descriptors shall apply:

/d0 Floppy Diskette Drive	Reserved name; no driver required
/f0 FLASH Drive	Accessed as RAM disk & OS-9/dd default Device
/h0 Hard Disk Drive	Reserved name; no drive required
/r0 FLASH RAM Drive	Accessed as RAM disk
/r1	Reserved; no driver required
/r2 Temporary DRAM Drive	Allows 1 MB of DRAM, accessed as RAM disk

2.6.2.3 A driver to handle each of the four internal timers under the OS-9 Kernel shall be provided. Access to the MC68360 internal timers shall be through SCFMAN using the following descriptors:

2.6.2.3.1 Descriptor names for each timer:

timer1 = access to MC68360's internal timer #1
timer2 = access to MC68360's internal timer #2
timer3 = access to MC68360's internal timer #3
timer4 = access to MC68360's internal timer #4
timer12 = access to MC68360's internal timer #1 & #2 [cascaded]
timer34 = access to MC68360's internal timer #3 & #4 [cascaded]

2.6.2.3.2 Timer Descriptor Option Structure

The driver shall change appropriate timer functions only and ignore values that do not apply to a particular timer function. The data structure is as follows:

```
typedef struct {

// Timer Global Configuration Register Related Options:
rserveTGCR :11; (MSB)
timerCAS :1; // Cascade timers
timerFRZ :1; // Freeze
timerSTP :1; // Stop timer
timerRST :1; // Reset timer
timerGM :1; // Gate mode                    default = 0 (LSB)

// Timer Mode Register Related Options:
```

```
timerPS :8; // Prescale value                    default = 0 (MSB)
timerCE :2; // Capture vdge & enable interrupts      default = 0
timerOM :1; // Output mode                       default = 0
timerORI :1; // Output reference interrupt enable     default = 0
timerFRR :1; // Free Run or Restart               default = 0
timerICLK :2; // Input Clock Source               default = 1
timerGE :1; // Gate Enable;                      default = 0 (LSB)

// Timer Reference Register
U_INT16 timerTRR                    default = 0

// Timer Capture Register
U_INT16 timerTCR                    default = 0xffff

// Timer Event Register
reserveTER :14; // Reserve (MSB)
timerREF :1; // Output reference event         default = 1
timerCAP :1; // Capture event          default = 1 (LSB)

} TTimer_opts;
```

2.6.2.3.3 Standard OS-9 SCFMAN Function Calls:

```
error_code _os_open (char *timer_desc_name, path_id *path);
error_code _os_close (path_id path);
error_code _os_gs_popt (path_id path, u_int32*sizeof(TTimer_opts), void
                        *timer_opts);
error_code _os_ss_popt (path_id path, u_int32*sizeof(TTimer_opts), void
                        *timer_opts);
error_code _os_write (path_id path, void *timer_value, 4);
error_code _os_read (path_id path, void *timer_value, 4);
```

2.6.2.4 The OS-9 SCFMAN and SPFMAN provided shall support each serial communication port with the protocols and data rates as specified.

2.6.2.6 The serial port drivers shall be software configurable to:

1.Enable/Disable hardware flow control (RTS/CTS)
2. Enable/Disable software flow control (XON/XOFF)
3. Set baud rate
4. Set data, parity, and stop bits
5. Change OS-9 Path Descriptor fields

The serial drivers shall support two hardware flow control modes: automatic and manual controls. The serial drivers shall operate in automatic mode when the serial port is opened. Upon receiving the first hardware flow control from

the user program, the serial driver shall operate in the manual mode until the serial port is closed. In the automatic mode and upon receipt of a write command, the serial drivers shall automatically raise RTS, then wait for CTS signal, then transmit data and finally drop RTS when the transmit buffer is emptied. In manual mode and upon the receipt of a write command, the serial drivers shall transmit data only when the RTS is raised by the user program and the CTS is asserted by the DCE. The serial driver shall stop data transmission as soon as the RTS is dropped by the user program.

In order to configure these features, the following calls shall be supported by the drivers:

GetStat Calls:
SS_Opt:
Get path options
SetStat Calls:
SS_Opt:
Set path options
SS_EnRTS:
Enable hardware modem control. The driver shall assert RTS continuously and not transmit unless CTS is asserted.
SS_DsRTS:
Disable hardware modem control. The driver shall de-assert RTS and ignore the start of CTS.

2.6.2.6 Four input buffering modes shall be provided:

1. Line - characters are buffered up to and including a programmable termination character.
2. Fixed - a fixed specified number of characters are buffered by the driver.
3. Timed - characters are buffered until a programmable inter-character time-out occurs.
4. Raw - characters are unbuffered & delivered to the task as received.

2.6.2.7 Line, Fixed, and Timed Modes shall be capable of being used together. Raw mode shall disable all other buffering modes.

2.6.2.8 Device drivers compliant with the OS-9 SCFMAN shall be provided for CPU Activity LED Indicator and Day Light Savings time correction features. The descriptor names shall be as follows:

led = access to CPU Activity LED Indicator
dstclock = access to Daylight Savings Time Clock correction

The standard OS-9 SCFMAN library calls and their functions are as follows:

```
error_code _os_open (char *desc_name, path_id *path);
                                //open descriptor for command
error_code _os_close (path_id path); //close descriptor
error_code _os_write (path_id path, void *value, 1);
                                //set value or function
*value = 1, turn led on or turn DLSclock feature on (default)
*value = 0, turn led off or turn DLSclock feature off
error_code _os_read (path_id path, void *value, 1);
                                //get current state
```

2.6.2.9 Time of Day (TOD) Clock

The OS-9 operating system's TOD Clock shall be driven by the LINESYNC derived OS-9 Operating System TICK Timer. The manufacturer shall provide the following features to support the TOD operation and synchronization.

2.6.2.9.1 The OS-9 System clock/calendar shall automatically be adjusted to account for DST and leap years, tracking years 1997 through 2017. A SCFMAN driver shall be provided to enable/disable the automatic DST adjustment.

2.6.2.9.2 A device driver compatible with the OS-9 SCFMAN shall be provided to allow the hardware TOD clock/calendar to be updated from the OS-9 system clock under application control. The descriptor name shall be "ClockUpdate." Opening the descriptor shall cause the driver to synchronize the clock to a minimum of 10 ms resolution. The driver shall compensate for any time elapsed during the process of updating the hardware clock.

2.6.2.9.3 At system power up, the OS-9 system TOD clock/calendar shall automatically be updated from the hardware TOD clock. The clocks shall by synchronized to a minimum of 10 ms resolution.

2.6.2.10 The FLASH RAM drive (/r0) shall be protected from corruption due to power failure during a write operation. The current sector of FLASH being written shall first be backed up in SRAM. The backup sector copy shall be invalidated when FLASH write operation is completed. In case of power failure, the FLASH driver shall detect the presence of the valid backup sector copy in SRAM and shall read sector data from the valid backup sector copy. A write operation shall restore the valid backup sector copy first. Execution of the program module, "FLRESTORE," in the Boot Image shall also restore the valid backup sector copy to FLASH drive after a specified delay. "FLRESTORE" shall accept a delay parameter in seconds ranging from 0 to 600 seconds. The default delay factor is 30 seconds. No more that 150 KB of SRAM shall be dedicated to this purpose.

2.6.3 Application Kernel

2.6.3.1 The provided software shall boot OS-9 from SYSRESET. The entire program shall be resident in FLASH Memory. The initialization routines shall configure the serial port protocols as follows:

SP1 & 2	1.2 Kbps, 8-bit word, 1 stop, no parity, no pause, no echo
SP 3	153.6 Kbps
SP 4	9.6 Kbps, 8-bit word, 1 stop, no parity, no pause
SP 5	614.4 Kbps
SP 6	38.4 Kbps, 8-bit word, 1 stop and no parity

2.6.3.2 Hardware initialization, preliminary self-test, OS-9 initialization (except Extended Memory Test), and forking OPEXEC shall be completed in less than 1.3 seconds.

2.6.3.3 A Trap Library routine, "Warmboot," shall be provided, which upon execution shall first shut down the OS-9 operating system, then jump to the start of the initialization routines executed on SYSRESET and proceed.

2.6.3.4 After initialization (boot up from SYSRESET), the program shall fork to the defined module in FLASH memory named OPEXEC preceded by a full path. If OPEXEC is not found or fails the program shall fork a shell. If OPEXEC is forked successfully, the program shall exit.

2.6.3.5 A Short Out is defined as the period of time between ACFAIL/POWER DOWN transition to LOW and back to HIGH without a SYSRESET transition to LOW. A Short Out results in resumption of Application Software without an operating system reboot. The Contractor shall provide a documented method for the Application Software to recover from Level 7 IRQ (ACFAIL) without a SYSRESET. A Long Out is defined as ACFAIL transition to LOW followed by a SYSRESET going LOW. The SYSRESET going HIGH shall be followed by an operating system reboot.

2.6.4 Error Handler

2.6.4.1 Error handling routine to cope with initialization and power-up test anomalies shall be provided. Errors that occur during initialization and/or during power-up test shall produce a report.

2.6.4.2 The Error Handler shall respond to the following conditions and generate an Error Report (saved in Memory):

1. Timer initialization error
2. Timer power up test error
3. Serial communication port initialization error
4. Serial communication port power up test error
5. Peripheral component initialization error

2.6.4.3 The Error Handler error report shall contain, at a minimum, component identification and an error code to identify the form of the error. The error report shall be a file accessible through the Random Block File Manager and named "ErrorReport."

2.6.5 Validation Suite

2.6.5.1 A validation suite of software and associated documentation shall be provided. It shall include all diagnostic programs necessary to test all 2070 UNIT functions. The diagnostic programs shall demonstrate that all software and hardware functions operate in conformance to specified functionality. It shall provide a working example of how to program all functions.

2.6.5.2 Validation suite software and associated documentation shall be segmented into individual test sequences. It shall be possible to separate out any one or group of these sequences and, with the addition of a general header file, execute it in isolation or in combination with application software.

2.6.5.3 When invoked, the validation suite shall run immediately after OS-9 has booted and shall execute in a continuous loop.

2.6.5.4 The validation suite shall execute as a task of the OS-9 Shell Utilities and Commands module. Execution from the shell shall be by typing "Valsuite" from the prompt. It shall be possible to execute the following additional CPU Module specific commands while in the OS-9 Shell Utility:

1. Get/Set the hardware time of day clock
2. Set OS-9 clock from hardware clock
3. Read/write all I/O registers internal to the MC 68360
4. Get/Set all programmable controls on serial ports
5. Verify that the 120 Hz interrupt is functioning
6. Set, configure, and read timers
7. Observe time-out interrupts

2.6.5.5 The OS-9 Shell Utility shall communicate with the user through the SP4 Port. When invoked, a low-priority task shall be executed for each SP port 1 and 2. Each task shall be configurable to use a different combination of input buffering options. The task shall open the port, configure it, and then enter a processing loop. In the loop, it shall wait for input and echo any input to the output. If no input is received for one second, an ASCII text string shall be sent out on the port. This text string shall be of the form *"port P hh:mm:ss."* P is the port number and hh:mm:ss is the current OS-9 time stamp. The text shall be terminated with a carriage return followed by a line feed character.

2.6.6 Deliverables

2.6.6.1 A software package resident on the FLASH Memory shall be provided, including the Embedded OS-9 kernels, platform drivers, and a validation suite.

2.6.6.2 All software shall be delivered in the following forms:

1. Contractor developed software with detailed manual (OS-9 not required)
2. Microware Ultra-C Version 1.1 compatible linkable object code
3. Memory map listing

2.6.6.3 Specific hardware memory addresses shall be specified and provided in a supplied INCLUDE FILE as defined constants. The INCLUDE FILE shall meet all applicable software delivery requirements.

2.6.6.4 Timer usage by drivers and their uninterrupted execution latencies, error values returned by driver calls, error codes, and a format of the error report file shall be documented.

2.6.6.5 Software to initialize and perform a power-up self-test of the CPU Module prior to the initialization of the OS-9 operating system shall be provided. All software components detailed in this specification or otherwise, and requiring initialization, shall be identified and the required initialization and nature of the test, documented. In addition, software provided to perform initialization and/or test shall be documented.

2.6.6.6 OS-9 compliant header files shall be provided with all Driver Modules.

2.7 National Transportation Communications for ITS Protocol (NTCIP) Compliance

The National Transportation Communications for ITS Protocol (NTCIP) TS 3.5-1996 Object Definitions for Actuated Traffic Signal Controller Units is not applicable until the Florida NTCIP ASC MIB is adopted. The Florida ASC MIB is currently under development.

NOTE: The manufacturer shall allow the use of any and all of this documentation by any party authorized by the Florida Department of Transportation for systems integration purposes at any time initially or in the future, regardless of what parties are involved in the systems integration effort.

SECTION 3 - MODEL 2070-2 FIELD I/O MODULE

3.1 Field I/O Module

The TYPE 2070-2A Field I/O MODULE (FI/O)shall consist of the Field Controller Unit; Parallel Input/Output Ports; other Module Circuit Functions (includes muzzle switch); Serial Communication Circuitry; Module Connectors C1S, C11S, and C12S mounted on the module front plate; VDC Power Supply (+12VDC to +5VDC); and required resident software.

3.3 Field Controller Unit

The Field Controller Unit (FCU) shall include a programmable microprocessor/controller unit together with all required clocking and support circuitry. Operational software necessary to meet housekeeping and functional requirements shall be provided resident in socketed firmware.

3.4 Parallel I/O Ports

3.4.1 The I/O Ports shall provide 64 bits of input using ground-true logic. Each input shall be read logic "1" when the input voltage at its field connector input is less than 3.5 VDC, and shall be read logic "0" when either the input current is less than 100 µA or the input voltage exceeds 8.5 VDC. Each input shall have an internal pull-up to the Isolated +12 VDC and shall not deliver greater than 20 mA to a short circuit to ground.

3.4.2 The I/O Ports shall provide 64 bits of output. Each output written as a logic "1" shall have a voltage at its field connector output of less than 4.0 VDC. Each output written as a logic "0" shall provide an open circuit (1 megohm or more) at its field connector output. Each output shall consist of an open-collector capable of driving 40 VDC minimum and sinking 100 mA minimum. Each output circuit shall be capable of switching from logic "1" to logic "0" within 100 s when connected to a load of 100 K-Ohms minimum. Each output circuit shall be protected from transients of 10 ±2 µs duration, ±300 VDC from a 1 K-Ohm source, with a maximum rate of 1 pulse per second.

3.4.3 Each output shall latch the data written and remain stable until either new data is written or the active-low reset signal. Upon an active-low reset signal, each output shall latch a logic "0" and retain that state until a new writing. The state of all output circuits at the time of Power Up or in Power Down state shall be open. It shall be possible to simultaneously assert all outputs within 100 µs of each other. An output circuit state not changed during a new writing shall not glitch when other output circuits are updated.

3.5 Other Module Circuit Functions

3.5.1 A maximum capacitive load of 100 pF shall be presented to the LINESYNC input signal. The EIA-485 compliant differential LINESYNC signals shall be derived from the LINESYNC signal.

3.5.2 A External WDT "Muzzle" Jumper shall be provided on the board. With the jumper in and NRESET transitions HIGH (FCU active), the FCU shall output a state change on Output Port 5, bit 8 (Connector C1, pin 103 – Monitor Watchdog Timer Input) every 100 ms for 3.5 seconds or due to CPU Command. When the jumper is missing (open), the feature shall not apply. This feature is required to operate with the Type 210 Monitor Unit only.

3.5.3 A WATCHDOG Circuit shall be provided. It shall be software enabled. Its enabled state shall be machine readable and reported in the FI/O status byte. Once enabled, the watchdog timer shall not be disabled without resetting the FI/O. The watchdog circuit shall have a range of 100 ms to 1 second. Failure of the FI/O to reset the watchdog timer within the prescribed timeout shall result in a hardware reset.

3.5.4 A synchronizable 1 KHz time reference shall be provided. It shall maintain a frequency accuracy of ±0.01% (±0.1 counts per second).

3.5.5 A 32-bit Millisecond Counter (MC) shall be provided for "timestamping." Each 1 KHz reference interrupt shall increment the MC.

3.5.6 At Power Up, the FCU loss of communications timer shall be extended to 3.5 seconds in lieu of 2 seconds.

3.5.7 A LOGIC Switch shall be provided resident on the module board. The switch shall function to disconnect Serial Port 3 (SP3) from the external world, Connector C12S. Its purpose is to prevent multiple use of SP3. A LED shall be provided on the module front panel labeled "SP3 ON". If LED light ON, SP3 is active and available at C12S.

3.6 Serial Communication Circuitry

3.6.1 System Serial Port 5 (SP5) EIA-485 signal lines shall enter the I/O Module and be split into two multi-drop isolated ports. One shall be routed to the FCU and the other converted to EIA-485, then routed to Connector C12S.

3.6.2 System Serial Port 3 (SP3) EIA-485 signal lines shall enter the I/O module and be isolated, converted back to EIA-485 and then routed to connector C12S.

3.6.3 LINE SYNC and POWER DOWN lines shall be split and isolated, one routed to the FCU for shut down functions and the other changed to EIA-485; then routed to connector C12S for external module use.

3.6.4 CPU RESET and POWER UP (SYSRESET) lines shall be isolated and "OR'd" to form NRESET. NRESET shall be used to reset FCU and other module devices. NRESET shall also be converted to EIA-485 then routed to connector C12S.

3.6.5 If the 2070 module is a –2B, then routing to FCU doesn't apply.

3.6.6 Isolation is between internal +5 VDC / Ground #1 and +12 VDC ISO / VDC Ground #2.

3.7 Buffers

A Transition Buffer shall be provided capable of holding a minimum of 1024 recorded entries. The Transition Buffer shall default to empty. There shall be two entry types: Transition and Rollover. The inputs shall be monitored for state transition. At each transition, a transition entry shall be added to the Transition Buffer. The MC shall be monitored for rollover. At each rollover transition ($xxxx FFFF - $xxxx 0000), a rollover entry shall be added to the Transition Buffer. For rollover entries, all bits of byte 1 are set to indicate that this is a rollover entry. Transition Buffer blocks are sent to the CPU module upon command. Upon confirmation of their reception, the blocks shall be removed from the Transition Buffer. The entry types are depicted as follows:

Input Transition Entry									
Description	**msb**							**lsb**	**Byte Number**
Transition Entry Identifier	S	Input Number							1
Timestamp NLSB	x	x	x	x	x	x	x	x	2
Timestamp LSB	x	x	x	x	x	x	x	x	3

Millisecond Counter Rollover Entry									
Description	**msb**							**lsb**	**Byte Number**
Transition Entry Identifier	1	1	1	1	1	1	1	1	1
Timestamp MSB	x	x	x	x	x	x	x	x	2
Timestamp NMSB	x	x	x	x	x	x	x	x	3

3.8 I/O Functions

3.8.1 Inputs

Input scanning shall begin at I0 (bit 0) and proceed to the highest input, ascending from lsb to msb. Each complete input scan shall finish within 100 µs. Once sampled, the logic state of an input shall be held until the next input scan. Each input shall be sampled 1,000 times per second. The time interval between samples shall be 1 ms ±100 µs. If configured to report, each input that has transitioned since its last sampling shall be identified by input number, transition state, and timestamp (at the time the input scan began) and shall be added as an entry to the Transition Buffer. If

multiple inputs change state during one input sample, these transitions shall be entered into the Input Transition Buffer by increasing number. The MC shall be sampled within 10 µs of the completion of the input scan.

3.8.2 Data Filtering

If configured, the inputs shall be filtered by the FCU to remove signal bounce. The filtered input signals shall then be monitored for changes as noted. The filtering parameters for each input shall consist of Ignore Input Flag and the On and Off filter samples. If the Ignore Input flag is set, no input transitions shall be recorded. The On and Off filter samples shall determine the number of consecutive samples an input must be on and off, respectively, before a change of state is recognized. If the change of state is shorter than the specified value, the change of state shall be ignored. The On and Off filter values shall be in the range of 0 to 255. A filter value of 0, for either or both values, shall result in no filtering for this input. The default values for input signals after reset shall be as follows:

Filtering	Enabled
On and off filter values shall be set to	5
Transition monitoring	Disabled (Timestamps are not logged)

3.8.3 Outputs

Simultaneous assertion of all outputs shall occur within 100 µs. Each output shall be capable of being individually configured in state to ON, OFF, or a state synchronized with either phase of LINESYNC. The condition of the outputs shall only be "ON" if the FI/O continues to receive active communications from the CPU Module. If there is no valid communications with the CPU Module for 2.0 seconds, all outputs shall revert to the OFF condition, and the FI/O status byte shall be updated to reflect the loss of communication from the CPU Module.

3.8.4 Standard Function

Each output shall be controlled by the data and control bits in the CPU Module-FI/O frame protocol as follows:

Output Bit Translation			
Case	Output Data Bit	Output Control Bit	Function
A	0	0	Output put in the OFF state
B	1	1	Output is a square wave, synchronized to the LINESYNC signal. When LINESYNC is ON (1), the output is OFF, and when LINESYNC is OFF (0), the output is ON.
C	0	1	Output is a square wave, synchronized to the LINESYNC signal. When LINESYNC is ON (1), the output is ON, and when LINESYNC is OFF (0), the output is OFF
D	1	0	Output is in the ON state

3.8.4.1 In Case A above, the corresponding output shall be turned OFF if previously ON and if previously OFF remain OFF until otherwise configured. For half-cycle switching (cases B and C), all outputs to be changed shall be changed within 50 µs after the corresponding LINESYNC transition and shall remain in the same state during the entire half cycle. In Case D above, the corresponding output shall be turned ON if previously OFF and if previously ON remain ON until otherwise configured. All outputs shall not glitch nor change state unless configured to do so.

3.8.5 Interrupts

All interrupts shall be capable of asynchronous operation with respect to all processing and all other interrupts. MILLISECOND Interrupt shall be activated by the 1 KHz reference once per ms. A timestamp rollover flag set by MC rollover shall be cleared only on command. LINESYNC Interrupt - This interrupt shall be generated by both the 0-1 and 1-0 transitions of the LINESYNC signal. The LINESYNC interrupt shall monitor the MC interrupt and set the MC error flag if there has not been an interrupt from the 1 KHz source for 0.5 seconds ($\geq$60 consecutive LINESYNC interrupts). The LINESYNC interrupt shall synchronize the 1 KHz time reference with the 0-1 transition of the LINESYNC signal once a second. A LINESYNC error flag shall be set if the LINESYNC interrupt has not successfully executed for 0.5 seconds or longer ($\geq$500 consecutive millisecond interrupts).

3.8.6 Communication Service Routine

A low-level communication service routine shall be provided to handle reception, transmission, and EIA-485 communication faults. The communication server shall automatically:

<u>For Transmission</u>:

- Generate the opening and closing flags
- Generate the CRC value
- Generate the abort sequence (minimum of 8 consecutive '1' bits) when commanded by the FCU
- Provide zero bit insertion

<u>For Receiving:</u>

- Detect the opening and closing flags
- Provide address comparison, generating an interrupt for messages addressed to the I/O Module, and ignoring messages not addressed to the I/O Module
- Strip out inserted zeros
- Calculate the CRC value, compare it to the received value, and generate an interrupt on an error
- Generate an interrupt if an abort sequence is received

3.8.7 Communication Processing

The priority one (highest) task shall be to process the command messages received from the CPU Module, prepare, and start response transmission. The response message transmission shall begin within 4 ms of the receipt of the received message. Message type processing time constraints shall not exceed 70 ms per message.

3.8.8 Input Processing

This priority two task shall process the raw input data scanned in by the 1 ms interrupt routine, perform all filtering, and maintain the transition queue entries.

3.9 DATA Communication Protocols

3.9.1 Protocols

All communication with the CPU Module shall be SDLC-compatible command-response protocol, support 0 bit stuffing, and operate at a data rate of 614.4 Kbps. The CPU Module shall always initiate the communication and should the command frame be incomplete or in error, no FI/O response shall be transmitted. The amount of bytes of a command or response is dependent upon the I/O Module identification.

3.9.1.1 The frame type shall be determined by the value of the first byte of the message. The command frames type values $70 - $7F and associated response frame type values $F0 - $FF are allocated to the Contractor diagnostics. All other frame types not called out are reserved. The command-response Frame Type values and message times shall be as follows:

Frame Types				
Module Command	**I/0 Module Response**	**Description**	**Minimum Message Time**	**Maximum Message Time**
49	177	Request Module Status	250 µs	275 µs
50	178	MILLISECOND CTR. Mgmt.	222.5 µs	237.5 µs
51	179	Configure Inputs	344.5 µs	6.8750 ms
52	180	Poll Raw Input Data	317.5 µs	320 µs
53	181	Poll Filtered Input Data	317.5 µs	320 µs
54	182	Poll Input Transition Buffer	300 µs	10.25 ms
55	183	Command Outputs	405 µs	410 µs
56	184	Config. Input Tracking Functions	340 µs	10.25 ms
57	185	Config. Complex Output Functions	340 µs	6.875 ms
58	186	Configure Watchdog	222.5 µs	222.5 µs
59	187	Cabinet Identification	222.5 µs	222.5 µs
60	188	I/O Module Identification	222.5 µs	222.5 µs
61-62	189-190	Reserved (note below)		
63	191	Poll variable length raw input	317.5 µs	320 µs
64	192	Variable length command outputs	405 µs	410 µs

3.9.1.2 Messages 61 / 189 and 62 / 190 are for ITS Cabinet Monitor Unit. See ITS Cabinet Monitor System Serial Bus #1 for Command and Response Frames (pending TEES Chapter 7). Message 63 / Message 191 shall be the same as Message 52 / 180 except Byte 2 of Message 180 response shall denote the following number of inputs bytes. Message 64 / 192 shall be the same as Message 55 / 183 except Byte 2 of the Message 55 Command shall denote the number of output data bytes along with the following output data.

3.9.2 Request Module Status

The Command shall be used to request FI/O status information response. Command/response frames are as follows:

Request Module Status Command									
Description	**msb**						**lsb**		**Byte Number**
(Type Number = 49)	0	0	1	1	0	0	0	1	Byte 1
Reset Status Bits	P	E	K	R	T	M	L	W	Byte 2

Request Module Status Response									
Description	**msb**						**lsb**		**Byte Number**
(Type Number = 177)	1	0	1	1	0	0	0	1	Byte 1
System Status	P	E	K	R	T	M	L	W	Byte 2
SCC Receive Error Count	Receive Error Count								Byte 3
SCC Transmit Error Count	Transmit Error Count								Byte 4
Timestamp MSB	Timestamp MSB								Byte 5
Timestamp NMSB	Timestamp NMSB								Byte 6
Timestamp NLSB	Timestamp NLSB								Byte 7
Timestamp LSB	Timestamp LSB								Byte 8

3.9.2.1 The response status bits are defined as follows:

P - Indicates FI/O hardware reset
E - Indicates a communications loss of greater than 2 seconds
M - Indicates an error with the MC interrupt
L - Indicates an error in the LINESYNC
W - Indicates that the FI/O has been reset by the Watchdog
R - Indicates that the EIA-485 receive error count byte has rolled over
T - Indicates that the EIA-485 transmit error count byte has rolled over
K - Indicates the Datakey has failed or is not present

3.9.2.2 Each of these bits shall be individually reset by a '1' in the corresponding bit of any subsequent Request Module Status frame, and the response frame shall report the current status bits. The SCC error count bytes shall not be reset. When a count rolls over (255 - 0), its corresponding roll-over flag shall be set.

3.9.3 MC Management

MC Management frame shall be used to set the value of the MC. The 'S' bit shall return status '0' on completion or '1' on error. The 32-bit value shall be loaded into the MC at the next 0-1 transition of the LINESYNC signal. The frames are as follows:

Millisecond Counter Management Command									
Description	**msb**						**lsb**		**Byte Number**
(Type Number = 50)	0	0	1	1	0	0	1	0	Byte 1
New Timestamp MSB	x	x	x	x	x	x	x	x	Byte 2
New Timestamp NMSB	x	x	x	x	x	x	x	x	Byte 3
New Timestamp NLSB	x	x	x	x	x	x	x	x	Byte 4
New Timestamp LSB	x	x	x	x	x	x	x	x	Byte 5

Millisecond Counter Management Response									
Description	**msb**						**lsb**		**Byte Number**
(Type Number = 178)	1	0	1	1	0	0	1	0	Byte 1
Status	0	0	0	0	0	0	0	S	Byte 2

3.9.4 Configure Inputs

The Configure Inputs command frame shall be used to change input configurations. The command-response frames are as follows:

Configure Inputs Command									
Description	**msb**						**lsb**		**Byte Number**
(Type Number = 51)	0	0	1	1	0	0	1	1	Byte 1
Number of Items (n)	n	n	n	n	n	n	n	n	Byte 2
Item # - Byte 1	E	Input Number							Byte 3(I-1)+3
Item # - Byte 2	Leading edge filter (e)								Byte 3(I-1)+4
Item # - Byte 3	Trailing edge filter (r)								Byte 3(I-1)+5

Configure Inputs Response									
Description	**msb**						**lsb**		**Byte Number**
(Type Number = 179)	1	0	1	1	0	0	1	1	Byte 1
Status	0	0	0	0	0	0	0	S	Byte 2

3.9.4.1 Block field definitions shall be as follows:

E - Ignore Input Flag. "1" = do not report transitions for this input, "0" = report transitions for this input

e - A one-byte leading edge filter specifying the number of consecutive input samples which must be "0" before the input is onsidered to have entered to "0" state from "1" state (range 1 to 255, 0 = disabled)

r - A one-byte trailing edge filter specifying the number of consecutive input samples which must be "1" before the input is considered to have entered to "1" state from "0" state (range 1 to 255, 0 = disabled)

S - return status S = '0' on completion or '1' on error

3.9.5 Poll Raw Input Data

The Poll Raw Input Data frame shall be used to poll the FI/O for the current unfiltered status of all inputs. The response frame shall contain 15 bytes of information indicating the current input status. The frames are as follows:

Poll Raw Input Data Command									
Description	**msb**						**lsb**		**Byte Number**
(Type Number = 52)	0	0	1	1	0	1	0	0	Byte 1

Poll Raw Input Data Response									
Description	**msb**						**lsb**		**Byte Number**
(Type Number = 180)	1	0	1	1	0	1	0	0	Byte 1
Inputs I0 (lsb) to I7 (msb)	x	x	x	x	x	x	x	x	Byte 2

Inputs I8 to I119	x	x	x	x	x	x	x	x	Bytes 3 to 16
Timestamp MSB	x	x	x	x	x	x	x	x	Byte 17
Timestamp NMSB	x	x	x	x	x	x	x	x	Byte 18
Timestamp NLSB	x	x	x	x	x	x	x	x	Byte 19
Timestamp LSB	x	x	x	x	x	x	x	x	Byte 20

3.9.6 Poll Filtered Input Data

The Poll Filtered Input Data frame shall be used to poll the FI/O for the current filtered status of all inputs. The response frame shall contain 15 bytes of information indicating the current filtered status of the inputs. Raw input data shall be provided in the response for inputs that are not configured for filtering. The frames are as follows:

Poll Filter Input Data Command									
Description	**msb**						**lsb**		**Byte Number**
(Type Number = 53)	0	0	1	1	0	1	0	1	Byte 1

Poll Filter Input Data Response									
Description	**msb**						**lsb**		**Byte Number**
(Type Number = 181)	1	0	1	1	0	1	0	1	Byte 1
Inputs I0 (lsb) to I7 (msb)	x	x	x	x	x	x	x	x	Byte 2
Inputs I8 to I119	x	x	x	x	x	x	x	x	Bytes 3 to 16
Timestamp MSB	x	x	x	x	x	x	x	x	Byte 17
Timestamp NMSB	x	x	x	x	x	x	x	x	Byte 18
Timestamp NLSB	x	x	x	x	x	x	x	x	Byte 19
Timestamp LSB	x	x	x	x	x	x	x	x	Byte 20

3.9.7 Poll Input Transition Buffer

The Poll Input Transition Buffer frame shall poll the FI/O for the contents of the system status queue. The response frame shall include a three-byte information field for each of the input changes that have occurred since the last interrogation. The frames are as follows:

Poll Input Transition Buffer Command									
Description	**msb**						**lsb**		**Byte Number**
(Type Number = 54)	0	0	1	1	0	1	1	0	Byte 1
Block Number	x	x	x	x	x	x	x	x	Byte 2

Poll Input Transition Buffer Response									
Description	**msb**						**lsb**		**Byte Number**
(Type Number = 182)	1	0	1	1	0	1	1	0	Byte 1
Block Number	x	x	x	x	x	x	x	x	Byte 2
Number of Entries	x	x	x	x	x	x	x	x	Byte 3
Item #	S	Input Number							Byte 3(I-1)+4
Item # Timestamp NLSB	x	x	x	x	x	x	x	x	Byte 3(I-1)+5

Item # Timestamp LSB	x	x	x	x	x	x	x	x	Byte 3(I-1)+6
Status	0	0	0	0	C	F	E	G	Byte 3(I-1)+7
Timestamp MSB	x	x	x	x	x	x	x	x	Byte 3(I-1)+8
Timestamp NMSB	x	x	x	x	x	x	x	x	Byte 3(I-1)+9
Timestamp NLSB	x	x	x	x	x	x	x	x	Byte 3(I-1)+10
Timestamp LSB	x	x	x	x	x	x	x	x	Byte 3(I-1)+11

3.9.7.1 Each detected state transition for each active input (see configuration data) is placed in the queue as it occurs. Queue byte entry definitions are as follows:

S - Indicates the state of the input after the transition
C - Indicates the 255 entry buffer limit has been exceeded
F - Indicates the 1024 buffer limit has been exceeded
G - Indicates the requested block number is out of monotonic increment sequence
E - Same block number requested, E is set in response

3.9.7.2 The Block Number byte is a monotonically increasing number incremented after each command issued by the CPU Module. When the FI/O Module receives this command, it shall compare the associated Block Number with the Block Number of the previously received command. If it is the same, the previous buffer shall be re-sent to the CPU Module and the 'E' flag set in the status response frame. If it is not equal to the previous Block Number, the old buffer shall be purged and the new data sent. If the block number is not incremented by one, the status G bit shall be set and the data of the requested block shall be sent. The Block Number byte sent in the response block shall be the same as that received in the command block. Counter rollover shall be considered as a normal increment.

3.9.8 Set Outputs

The Set Outputs frame shall be used to command the FI/O to set the Outputs according to the data in the frame. If there is any error configuring the outputs, the 'E' flag in the response frame shall be set to '1'. If the LINESYNC reference has been lost, the 'L' bit in the response frame shall be set. Loss of LINESYNC reference shall also be indicated in system status information. These command and response frames are as follows:

Set Outputs Command									
Description	**msb**						**lsb**		**Byte Number**
(Type Number = 55)	0	0	1	1	0	1	1	1	Byte 1
Outputs O0 (lsb) to O7 (msb) Data	x	x	x	x	x	x	x	x	Byte 2
Outputs O8 to O103 Data	x	x	x	x	x	x	x	x	Bytes 3 to 14

Outputs O0 (lsb) to O7 (msb) Control	x	x	x	x	x	x	x	x	Byte 15
Outputs O8 to O103 Control	x	x	x	x	x	x	x	x	Bytes 16 to 27

Set Outputs Response									
Description	**msb**						**lsb**		**Byte Number**
(Type Number = 183)	1	0	1	1	0	1	1	1	Byte 1
Status	0	0	0	0	0	0	L	E	Byte 2

3.9.9 Configure Input Tracking Functions

The Configure Input Tracking Functions frame shall be used to configure outputs to respond to transitions on a specified input. Each Output Number identified by Item Number shall respond as configured to the corresponding Input Number identified by the same Item Number. Input to Output mapping shall be one to one. If a command results in more than 8 input tracking outputs being configured, the response V bit shall be set to ‘1’ and the command shall not be implemented. The command and response frames are as follows:

Configure Input Tracking Functions Command									
Description	**msb**						**lsb**		**Byte Number**
(Type Number = 56)	0	0	1	1	1	0	0	0	Byte 1
Number of Items	Number of Items								Byte 2
Item # - Byte 1	E	Output Number							Byte 2(I-1)+3
Item # - Byte 2	I	Input Number							Byte 2(I-1)+4

Configure Input Tracking Functions Response									
Description	**msb**						**lsb**		**Byte Number**
(Type Number = 184)	1	0	1	1	1	0	0	0	Byte 1
Status	0	0	0	0	0	0	0	V	Byte 2
Timestamp MSB	x	x	x	x	x	x	x	x	Byte 3
Timestamp NMSB	x	x	x	x	x	x	x	x	Byte 4
Timestamp NLSB	x	x	x	x	x	x	x	x	Byte 5
Timestamp LSB	x	x	x	x	x	x	x	x	Byte 6

3.9.9.1 Definitions are as follows:

E '1’ - Enable input tracking functions for this output
'0' - Disable input tracking functions for this output
I '1' - The output is OFF when input is ON, ON when input OFF
'0' - The output is ON when input is ON, OFF when input is OFF
V '1' - The max. number of 8 configurable outputs has been exceeded
'0' - No error
Number of Items - The number of entries in the frame. If zero, all outputs currently configured for input tracking shall be disabled.

3.9.9.2 The timestamp value shall be sampled prior to the response frame.

3.9.9.3 Outputs which track inputs shall be updated no less than once per ms. Input to output signal propagation delay shall not exceed 2 ms.

3.9.9.4 The “Number of Item” field is valid from 0 to 16 (most that is sent at one time is 8 enables and 8 disables). If processing a command resulting in more than 8 Input Tracking functions being enabled, none of the command shall be implemented and response message “V” bit set to 1. If an invalid output or input number is specified for a function, the FIOM software shall not do that function definition. It shall also not be counted toward the maximum of 8 input tracking function allowed. The rest of the message shall be processed. When an Input Tracking function is disabled, the output is set according to the most recently received Set Outputs Command. When an input tracking function for an output is superseded (redefined as either another input tracking function, or as a complex output function) nothing shall be done with the output. The most recent value remains until the new function changes it.

3.9.10 Configure Complex Output Functions

The Configure Complex Output Functions frame shall be used to specify a complex output for one to eight of any of the outputs. If a Configure Complex Output Function command results in more than eight outputs being configured, the 'V' bit in the response message shall be set to a '1', and the command shall not be implemented. Two output forms shall be provided, single pulse and continuous oscillation. These output forms shall be configurable to begin immediately or on a specified input trigger and, in the case of continuous oscillation, to continue until otherwise configured or to oscillate only while gated active by a specified input. If the command gate bit is active, the command trigger bit shall be ignored and the specified input shall be used as a gate signal. The command and response frames are as follows:

Configure Complex Output Functions Command									
Description	**msb**							**lsb**	**Byte Number**
(Type Number = 57)	0	0	1	1	1	0	0	1	Byte 1
Number of Items	Number of Items								Byte 2
Item # - Byte 1	0	Output Number							Byte 7(I-1)+3
Item # - Byte 2	Primary Duration (MSB)								Byte 7(I-1)+4
Item # - Byte 3	Primary Duration (LSB)								Byte 7(I-1)+5
Item # - Byte 4	Secondary Duration (MSB)								Byte 7(I-1)+6
Item # - Byte 5	Secondary Duration (LSB)								Byte 7(I-1)+7
Item # - Byte 6	0	Input Number							Byte 7(I-1)+8
Item # - Byte 7	P	W	G	E	J	F	R	L	Byte 2(I-1)+4

Configure Complex Output Functions Response									
Description	**msb**						**lsb**		**Byte Number**
(Type Number = 185)	1	0	1	1	1	0	0	1	Byte 1

Status	0	0	0	0	0	0	0	V	Byte 2
Timestamp (MSB)	x	x	x	x	x	x	x	x	Byte 3
Timestamp (NMSB)	x	x	x	x	x	x	x	x	Byte 4
Timestamp (NLSB)	x	x	x	x	x	x	x	x	Byte 5
Timestamp (LSB)	x	x	x	x	x	x	x	x	Byte 6

3.9.10.1 The bit fields of the command frame are defined as follows:

E '1' - enable complex output function for this output
'0' - disable complex output function for this output

J '1' - During the primary duration, the output shall be written as a logic '1'. During the secondary duration, the output shall be written as a logic '0'.
'0' - During the primary duration, the output shall be written as a logic '0'. During the secondary duration, the output shall be written as a logic '1'.

Output Number - 7-bit output number identifying outputs

Primary Duration - For single pulse operation, this shall determine the number of 'ticks' preceding the pulse. For continuous oscillation, this shall determine the length of the inactive (first) portion of the cycle.

Secondary Duration - For single pulse operation, this shall determine the number of 'ticks' the pulse is active. Subsequent to the secondary duration, the output shall return to the state held previous to the primary duration. For continuous oscillation, this shall determine the length of the active (second) portion of the cycle. 0 = hold output state until otherwise configured.

F '1' - The trigger or gate shall be acquired subsequent to filtering the specified input. The raw input signal shall be used if filtering is not enabled for the specified input.
'0' - The trigger or gate shall be derived from the raw input.

R '1' - For triggered output, the output shall be triggered by an ON-to-OFF transition of the specified input and shall be triggered immediately upon command receipt if the input is OFF. For gated output, the output shall be active while the input is OFF.
'0' - For triggered output, the output shall be triggered by an OFF- o-ON transition of the specified input and shall be triggered immediately upon command receipt if the input is ON. For gated output, the output shall be active while the input is ON.

Input Number - 7-bit input number identifying inputs 0 Up.

P '1' - The output is configured for single-pulse operation. Once complete, the complex output function shall be disabled.
'0' - The output is configured for continuous oscillation.

W '1' - It is triggered by the specified input. Triggered complex output shall commence within 2 ms of the associated trigger.
'0' - Operation shall begin within 2 ms of the command receipt.

G '1' - Operation shall be gated active by the specified input.
'0' - Gating is inactive.

L '1' - The LINESYNC based clock shall be used for the time ticks.
'0' - The MC shall be used for the time ticks.

V '1' - Indicates maximum number of configurable outputs is exceeded.
'0' - No error

Number of items - The number of entries in the frame. If 0, all outputs currently configured as complex outputs shall be disabled. 3.9.10.2 Controlling input signals shall be sampled at least once per millisecond.

3.9.10.2 Controlling input signals shall be sampled at least once per millisecond.

3.9.10.3 The “Number of Items” field is valid from 0 to 16. Zero means disable all Complex Output functions. Sixteen is the maximum because the most that is sent at one time is 8 enables and 8 disables. If processing a command results in more than 8 Complex Output functions being enabled, none of the command shall be implemented and the response message “V” bit shall be set to 1. If an invalid output or input number (the “G” or “W” bits being set to 1) is specified for a function, that function definition is not done by the FIOM software. It shall also not be counted towards the maximum of 8 Complex Output functions allowed. The rest of the message shall be processed. When a Complex Output function is disabled, the output is set according to the most recently received Set Outputs command. When a complex output function for an output is superseded, that is, redefined as wither another Complex Output function, or as an Input Tracking function, nothing special is done with the output. The most recent value remains until the new function changes it. The “G” bit (gating) set to 1 takes precedence over the “W” bit (triggering). If gating is ON, triggering is turned OFF, regardless of the value of the “W” bit in the command message. If a Complex Output is configured with the “G” bit set to 1 (gating) and the “P” bit set to 0 (continuous oscillation), the output is set to OFF (0) whenever the specified input changes state so that the oscillation should cease (output inactive). For a single pulse operation (“G” bit set to 1), after the secondary duration completes the

Complex Output function shall be disabled, and the output shall be set according to the most recently received Set Outputs command.

3.9.11 Configure Watchdog

The Configure Watchdog frames shall be used to enable the software watchdog and to set it's timeout value. The Command and response frames are as follows:

Configure Watchdog Command									
Description	**msb**						**lsb**		**Byte Number**
(Type Number = 58)	0	0	1	1	1	0	1	0	Byte 1
Timeout Value	x	x	x	x	x	x	x	x	Byte 2

Configure Complex Output Functions Response									
Description	**msb**						**lsb**		**Byte Number**
(Type Number = 186)	1	0	1	1	1	0	1	0	Byte 1
Status	0	0	0	0	0	0	0	Y	Byte 2

3.9.11.1 The timeout value shall be in the range between 10 to 100 ms. If the value is lower than 10, 10 shall be assumed. If the value is greater than 100, 100 shall be assumed.

3.9.11.2 On receipt of this frame, the watchdog timeout value shall be changed to the value in the message and the “Y” bit set. The response frame bit (Y) shall indicate a '1' if the watchdog has been previously set and a '0' if not.

3.9.12 Cabinet Identification

The Cabinet Identification Command frame shall be used to request the cabinet identification response frame containing all 128 bytes stored in the Datakey. On power restoration and immediately prior to any interrogation of the Datakey, the FI/O shall test for the presence of the Datakey. If absent, the FI/O status K bit shall be set and no interrogation shall take place. If an error occurs during interrogation, FI/O status K bit shall be set. The command and response frames are as follows:

Cabinet Identification Command									
Description	**msb**						**lsb**		**Byte Number**
(Type Number = 59)	0	0	1	1	1	0	1	1	Byte 1

Cabinet Identification Response									
Description	**msb**						**lsb**		**Byte Number**
(Type Number = 187)	1	0	1	1	1	0	1	1	Byte 1
Status	0	0	0	0	0	0	0	K	Byte 2
Datakey (128 Bytes)	x	x	x	x	x	x	x	x	Bytes 3 - 130

3.9.13 Module Identification

The FI/O Identification command frame shall be used to request the FI/O Identification value Response of "1" for the 2070-2A, "2" for the 2070-8 FI/O, and "3" for ITS Cabinets. The command and response frames are shown as follows:

I/O Module Identification Command									
Description	**msb**						**lsb**		**Byte Number**
(Type Number = 60)	0	0	1	1	1	1	0	0	Byte 1

I/O Module Identification Response									
Description	**msb**						**lsb**		**Byte Number**
(Type Number = 186)	1	0	1	1	1	1	0	0	Byte 1
Status	x	x	x	x	x	x	x	x	Byte 2

SECTION 4 - MODEL 2070-3 FRONT PANEL ASSEMBLY

4.1 General

The Type 2070-3 Front Panel Assembly (FPA) shall be delivered with one of the three options. All options shall consist of a panel with Latch assembly and two TSD #1 hinge attaching devices, assembly PCB, external serial port connector(s), CPU active LED indicator, and FP Harness Interface. The options shall include the additional features, as follows:

OPTION A - FPA controller, two keyboards, AUX switch, alarm bell and Display A
OPTION B - FPA controller, two keyboards, AUX switch, alarm bell and Display B
OPTION C - (Blank) System Serial Port 6 Lines, isolated and vectored to Connector C60S.

4.2 Keyboards

Two KEYBOARDS shall be provided, one with sixteen keys for hexadecimal alphanumeric entry and the other with twelve keys to be used for cursor control and action symbol entry. Each key shall be engraved or embossed with its function character. Each key shall have an actuation force between 50 and 100 grams and provide a positive tactile indication of contact closure. Key contacts shall be hermetically sealed, have a design life of over one million operations, shall be rated for the current and voltage levels used, and shall stabilize within 5 ms following contact closure.

4.3 CPU Active Indicator

The cathode of the CPU Active LED Indicator shall be electrically connected to the CPU Activity LED signal and shall be pulled up to +5 VDC.

4.4 Display

The DISPLAY shall consist of a Liquid Crystal Display (LCD), a backlight, and a contrast potentiometer control. Display A shall have 4 lines of 40 characters each with a minimum character dimensions of 5.00 mm wide by 10.44 mm high and an electro - luminescent (EL) backlight. Display B shall have 8 lines of 40 characters each with minimum dimensions of 2.65 mm wide by 4.24 mm high and either LED or EL backlight.

4.4.1 Each character shall be composed of a 5 x 7 dot matrix with a underline row or a 5 x 8 dot matrix. The viewing angle of the LCD shall be optimized for direct (90°) viewing, +/-35° vertical, +/-45° horizontal. The LCD shall have variable contrast with a minimum ratio of 4:1. The LCD shall be capable of displaying, at any position on the Display, any of the standard ASCII characters as well as user-defined characters.

4.4.2 The backlight shall be turned on and off by the Controller Circuitry. The backlight and associated circuitry shall consume no power when in off state. A

potentiometer shall control the LCD contrast with clockwise rotation increasing contrast. The contrast shall depend on the angular position of the potentiometer, which shall provide the entire contrast range of the LCD.

4.4.3 Cursor display shall be turned ON and OFF by command. When ON, the cursor shall be displayed at the current cursor position. When OFF, no cursor shall be displayed. All other cursor functions (positioning, etc.) shall remain in effect.

4.5 FPA Controller

The FPA Controller shall function as the Front Panel Device controller interfacing with the CPU Module.

4.5.1 A FPA RESET Switch shall be provided on the Assembly PCB. The momentary CONTROL switch shall be in logic OR with the CPU RESET Line, producing a FPA RESET Output. Upon FPA RESET being active or receipt of a valid Soft Reset display command, the following shall occur:

1. Auto-repeat, blinking, auto-wrap, and auto-scroll shall be set to OFF.
2. Each special character shall be set to ASCII SPC (space).
3. The tab stops shall be set to columns 9, 17, 25, and 33.
4. The backlight timeout value shall be set to 6 (60 seconds).
5. The backlight shall be extinguished.
6. The display shall be cleared (all ASCII SPC).
7. The FPA module shall transmit a power up string through /sp6 to the CPU once power is applied to the FPA, or the FPA hardware RESET BUTTON IS PUSHED. The string is " ESC [PU", hex value "1B 5B 50 55".

4.5.2 When a keypress is detected, the appropriate key code shall be transmitted to SP6-RxD. If two or more keys are depressed simultaneously, no code shall be sent. If a key is depressed while another key is depressed, no additional code shall be sent.

4.5.3 Auto-repeat shall be turned ON and OFF by command. When ON, the key code shall be repeated at a rate of 10 times per second starting when the key has been depressed continuously for 0.5 second, and shall terminate when the key is released or another key is pressed.

4.5.4 When the AUX Switch is toggled, the appropriate AUX Switch code shall be transmitted to the CPU.

4.5.5 The controller circuitry shall be capable of composing and storing eight special graphical characters on command, and displaying any number of these characters in combination with the standard ASCII characters. Undefined characters shall be ignored. User-composed characters shall be represented in the communication protocol in **Section 3**. P1 represents the special character number (1-8). Pn's represent columns of pixels from left to right. The most significant bit of each Pn represents the

top pixel in a column and the least significant bit shall represent the bottom pixel. A logic ‘1’ shall turn the pixel ON. There shall be a minimum of 5 Pn's for 5 columns of pixels in a command code sequence terminated by an "f." If the number of Pn's is more than the number of columns available on the LCD, the extra Pn's shall be ignored. P1 and all Pn's shall be in ASCII coded decimal characters without leading zero.

4.5.6 Character overwrite mode shall be the only display mode supported. A displayable character received shall always overwrite the current cursor position on the Display. The cursor shall automatically move right one character position on the Display after each character write operation. When the rightmost character on a line (position 40) has been overwritten, the cursor position shall be determined based on the current settings of the auto-wrap mode.

4.5.7 Auto-wrap shall turned ON & OFF by command. When ON, a new line operation shall be performed after writing to position 40. When OFF, upon reaching position 40, input characters shall continue to overwrite position 40.

4.5.8 Cursor positioning shall be non-destructive. Cursor movement shall not affect the current display, other than blinking the cursor momentarily and periodically hiding the character at that cursor position.

4.5.9 Blinking characters shall be supported, and shall be turned ON and OFF by command. When ON, all subsequently received displayable characters shall blink at the rate of 1 Hz with a 60 % ON / 40 % OFF duty cycle. It shall be possible to display both blinking and non-blinking characters simultaneously.

4.5.10 Tab stops shall be configurable at all columns. A tab stop shall be set at the current cursor position when a SetTabStop command is received. Tab Stop(s) shall be cleared on receipt of a ClearTabStop command. On receipt of the HT (tab) code, the cursor shall move to the next tab stop to the right of the cursor position. If no tab stop is set to the right of the current cursor position, the cursor shall not move.

4.5.11 Auto-scroll shall be turned ON and OFF by command. When ON, a Line Feed or new line operation from the bottom line shall result in the display moving up one line. When OFF, a Line Feed or new line from the bottom line shall result in the top line clearing, and the cursor being positioned on the top line.

4.5.12 Displayable characters shall be displayed within 500 microseconds (s) after receipt of the character code.

4.5.13 The Display backlight shall illuminate when any key is pressed and shall illuminate or extinguish by command. The backlight shall extinguish when no key is pressed for a specified time. This time shall be selected by programming command, by a number in the range 0 to 63 corresponding to that number of 10-second intervals.

A value of 1 shall correspond to a timeout interval of 10 seconds. A value of 0 shall indicate no timeout.

4.5.14 The Command Codes shall use the following conventions:

1. Parameters and Options: Parameters are depicted in both the ASCII and hexadecimal representations as the letter 'P' followed by a lower-case character or number. These are interpreted as follows:

   Pn: Value parameter, to be replaced by a value
   P1: Ordered and numbered parameter. One of a listed known parameters with a specified order and number (Continues with P2, P3, etc.)
   Px: Display column number (1-40)
   Py: Display line (1-4)
   ...: Continue the list in the same fashion

   Values of 'h' ($68) and 'l' ($6C) are used to indicate binary operations. 'h' represents ON (high), 'l' represents OFF (low).

2. ASCII Representation: Individual characters are separated by spaces; these are not to be interpreted as the space character, which is depicted by SPC.

3. Hexadecimal Representation: Characters are shown as their hexadecimal values and will be in the range 00 to 7F (7 bits).

4.5.15 The Controller Circuit shall communicate via a SP6 asynchronous serial interface. The interface shall be configured for 38.4 Kbps, 8 data bits, 1 stop bit, and no parity.

4.5.16 C50 ENABLE function when grounded by pins 1 and 5, shall be brought to Connectors A1, pin B21 for the purpose of disabling the module channel 2, (SP4).

4.6 Electronic Bell

The Front Panel shall include an electronic bell to signal receipt of ^G (hex 07). The bell shall sound at 2,000 Hz, with a minimum output of 85 dB, for 250 ms upon receipt of ^G (hex 07). Receipt of all other characters and ESC codes shall continue during the time the bell sounds.

SECTION 5 - MODEL 2070-4 POWER SUPPLY MODULE

5.1 Power Supply Module

The Model 2070-4A Power Supply Module shall be an independent, self-contained module, rated at 10 Amp, vented, and cooled by convection only. The Module shall slide into the unit's power supply compartment from the back of the Chassis and be attached to the Backplane Mounting Surface by its four TSD #3 Devices.

5.2 Module Front

An "On/Off" POWER Switch, four LED DC Power Indicators, PS Receptacle POWER Connectors, and the Incoming AC Fuse protection shall be provided on the Module Front. The LED DC POWER Indicators shall indicate all required DC voltages meet the following conditions: the +5 VDC is within 5% and the 12 VDC is within 8% of their nominal levels.

5.3 Input Protection

Two 0.5-Ohm, 10-watt wire-wound power resistors with a 0.2 µH inductance shall be provided (one on the AC+ Line & on the AC- Line). Three 20 Joule surge arresters shall be provided between AC+ to AC-, AC+ to EG, and AC- to EG. A 0.68 µF capacitor shall be placed between AC+ & AC- (between the resistor & arresters).

5.4 Positive 5 VDC Standby Power

A positive 5 VDC Standby Power shall be provided to hold up specified circuitry during the power down period. It shall consist of the monitor circuitry, hold up capacitors, and charging circuitry. A charging circuit shall be provided, that under normal operation, shall fully charge and float the capacitors consistent with the manufacturers' recommendations. The Hold Up power requirements shall be a minimum constant drain of 600 µA at a range of +5 VDC to +2 VDC for over 600 minutes.

5.5 Monitor Circuitry

Monitor Circuitry shall be provided to monitor incoming AC Power for Power Failure and Restoration and LINESYNC generation.

5.5.1 The ACFAIL/POWER DOWN Output Lines shall go LOW (ground true) immediately upon Power Failure. The Lines shall transition to HIGH at Power Restoration. The Lines shall be driven separately. The SYSRESET/POWERUP Output Lines shall transition to LOW 525 +/-25 ms after ACFAIL/POWER DOWN transition to LOW. The Lines shall transition to HIGH 225 +/-25 ms after Power Restoration and the supply is fully recovered. The Lines shall be driven separately.

5.5.2 The monitor circuitry shall switch the +5 VDC Standby ON immediately upon Power Failure and isolate (OFF) the line at Power Up.

5.5.3 The 120 Hz Square Wave LINESYNC signal shall be generated by a 120-Hz crystal oscillator, which shall be synchronized (positive transition)to the 60-Hz VAC incoming power line at 120 and 300 degrees. A continuous square wave signal

shall be +5 VDC amplitude, 8.333 ms half-cycle pulse duration, and 50 ±1% duty cycle. The output shall have drive sink capability of 16 mA. A 2 K-Ohm pull-up resistor shall be connected between the output and +5 VDC. The monitor circuit shall compensate for missing pulses and line noise during normal operation.

5.5.4 The LINESYNC shall continue until SYSRESET transitions LOW and begin then SYSRESET transitions HIGH.

5.6 Power Supply Requirements

Voltage	Tolerances	I Minimum	I Maximum
+5 VDC	+4.875 to +5.125 VDC	1.0 AMP	10.0 AMP
+12 VDC Serial	+11.64 to +12.36 VDC	0.1 AMP	0.5 AMP
-12 VDC Serial	-11.64 to -12.36 VDC	0.1 AMP	0.5 AMP
+12 VDC	+11.64 to +12.36 VDC	0.1 AMP	1.0 AMP

5.6.1 Line Regulation

±1.0 % from 90 VAC to 135 VAC rms

5.6.2 Load Regulation

±1.0 % for +5 VDC at 20 to 100 % load & ±5.0 % for +12, +12 & -12 Serial VDC at 50 to 100 % load

5.6.3 Efficiency

70 % minimum

5.6.4 Ripple & noise

Less than 0.2 % rms, 1 % peak to peak, or 50mV, whichever is greater

5.6.5 Voltage Overshoot

No greater than 5 %, all outputs

5.6.6 Overvoltage Protection

130 % of the output voltage for every output

5.6.7 Overload & Short Circuit Protection

Power foldback point 120% of max rated power
Automatic recovery upon removal of fault

5.6.8 Inrush Current

Cold Start Inrush shall be less than 25A at 115VAC

5.6.9 Transient Response

Output voltage shall be back to within 1 % of the rated value in less than 500 µs on a 50 % Load change. Peak transient not to exceed 5 % of rated value.

5.6.10 Holdup Time

The power supply shall supply 30 watts minimum for 550 ms after ACFAIL going LOW. The supply shall be capable of holding up the Unit for two 500 ms Power Loss periods occurring in a 1.5-second period

5.6.11 Remote Sense

+5 VDC shall compensate 250mV total line drop. Open sense load protection shall be provided.

SECTION 6 - UNIT CHASSIS AND TYPE 2070-5 VME CAGE ASSEMBLY

6.1 Unit Chassis

The Chassis shall consist of the metal housing, Serial Motherboard, Back-plane Mounting Surface, Power Supply Module Supports, slot card guides, Wiring Harnesses, and Cover Plate(s).

6.1.1 Metal Housing

6.1.1.1 All external screws shall be countersunk and shall be Phillips flat head stainless steel type.

6.1.1.2 The housing shall be treated with clear chromate and the slot designation labeled on the back-plane mounting surface above the upper slot card guide.

6.1.1.3 The Chassis shall be cooled by convection only. The top and bottom pieces of the housing shall be slotted for vertical ventilation.

6.1.2 Serial Motherboard

The Serial Motherboard shall function as support for its connectors, H1 to H4 and FP, and as the interface between the CPU and the dedicated modules/Front Panel carrying both serial communications, logic, and power circuits. The PCB shall be multi-layered, with one layer plane assigned to DC Ground.

6.1.2.1 A wiring harness PS2 shall be provided between the Power Supply and the Serial Motherboard PCB (to provide strain relief). Test points shall be provided on the Front Panel Assembly (FPA) side of the Serial Motherboard for PS2 lines.

6.1.2.2 A wiring harness FP shall be provided, linking the Serial Motherboard with the FPA.

6.1.3 Type 2070-1A CPU Main Controller Board

The Type 2070-1A CPU Main Controller Board (MCB) shall either be affixed to the Transition Board via at least four stand-off devices. A PS1L Harness shall be supplied with one end mating to the PS1 power supply connector and the other end mated to the MCB DIN Connector. The VME bus lines shall be terminated by a 100-Ohm resistor per line.

6.2 Type 2070-5 VME Cage Assembly

TYPE 2070-5 VME CAGE ASSEMBLY shall consist of 3U five slot/connector VME Cage, Front Mounting Plate, and PS1 Harness. The VME Cage shall conform to VME Standard IEEE P1014/D12 for 3U Cage. All slot/connectors shall be A24:D16 Interface.

SECTION 7 - SERIAL COMMUNICATION MODULE

7.1 General

a) The 2070-6 ASYNC/MODEM SERIAL COMM MODULE and 2070-7 ASYNC SERIAL COMM MODULE shall provide circuitry to disable its Channels 1 and 2 signal lines when a ground-true state is presented at Hx Pin B22 (C60) and Hx Pin B21 (C50). The Disable line shall normally be pulled up on the module.
b) Line drivers/receivers shall be socket mounted.
c) Isolation circuitry shall be opto- or capacitive-coupled isolation technologies. Each module's circuit shall be capable of reliably passing a minimum of 1.0 Mbps.
d) The Comm modules shall be "Hot" swappable without damage to circuitry or operations.

7.2 Type 2070-6 A & B Async/Modem Serial Comm Modules

7.2.1 Power Requirements

A fused isolated +5 VDC with a minimum of 100 mA power supply shall be provided for external use.

7.2.2 Circuitry

Two circuits, designated CIRCUIT #1 and CIRCUIT #2, shall be provided. Both circuit functions shall be identical, except for their Serial Communications Port and external connector (CIRCUIT #1 to SP1 [or SP3] and C2S Connector and CIRCUIT #2 to SP2 [or SP4] and C20S Connector).

7.2.2.1 The Circuits shall convert the 2070 UNIT Motherboard SP EIA-485 signals to/from board TTL level signals, isolate and drive the converted EIA-232 Signals interfacing with their associated MODEM and external connector.

7.2.3 Modem Requirements

Each CIRCUIT shall have a MODEM with the following requirements:

a) Data Rate: Baud modulation of 300 to 1200 for Module 2070-6A and 0 to 9600 for Module 2070-6B.
b) Modulation: Phase coherent frequency shift keying (FSK).
c) Data Format: Asynchronous, serial by bit.
d) Line & Signal Requirements: Type 3002 voice-grade, unconditioned Tone Carrier Frequencies (Transmit and Receive):2070-6A - 1.2 KHz MARK and 2.2 KHz SPACE, ±1% tolerance. 2070-6B - 11.2 KHz MARK and 17.6 KHz SPACE, ±1% tolerance. The operating band shall be (half power, -3 dB) between 1.0 KHz & .4 KHz for 2070-6A and 9.9 KHz & 18.9 KHz for 2070-6B.
e) Transmitting Output Signal Level: 0, -2, -4, -6, and -8 dB (at 1.7 KHz for 2070-6A & 14.7 KHz for 2070-6B) continuous or switch selectable.
f) Receiver Input Sensitivity: 0 to -40 dB.

g) Receiver Bandpass Filter: Shall meet the error rate requirement specified below and shall provide 20 dB/octave, minimum active attenuation for all frequencies outside the operating band.
h) Clear-to-Send (CTS) Delay: 11 ±3 ms.
i) Receive Line Signal Detect Time: 8 ±2 ms mark frequency.
j) Receive Line Squelch: 6.5 (±1) ms, 0 ms (OUT).
k) Soft Carrier Turn Off Time: 10 ±2 ms (0.9 KHz for 2070-6A and 7.8 KHz for 2070-6B). When the RTS is unasserted , the carrier shall turn off or go to soft carrier frequency.
l) Modem Recovery Timer: Capable of receiving data within 22 ms after completion of transmission.
m) Error Rate: Shall not exceed 1 bit in 100 Kbits, with a signal-to-noise ratio of 16 dB measured with flat-weight over a 300 to 3,000 Hz band.
n) Transmit Noise: Less than -50 dB across 600-ohms resistive load within the frequency spectrum of 300 to 3,000 Hz at maximum output.
o) Modem interface: EIA-232 Standards.

7.2.4 Logic Switches

Two LOGIC switches per circuit shall be provided (faceplate mounted).

7.2.4.1 One shall be used to vertically switch between Half-Duplex (Down) and Full-Duplex (Up). In Half-Duplex mode, the Transmit connections shall be used for both Receive and Transmit.

7.2.4.2 A MODEM Enable switch shall be provided that when in the UP Position shall enable MODEM and disable MODEM in the DOWN Position.

7.2.5 Control Switch

A CONTROL switch shall be provided on the module front panel to turn ON (Up) / OFF (Down) all module power.

7.3 Type 2070-7A & 7B Async Serial Comm Module

7.3.1 Circuitry

Two circuits, designated CIRCUIT #1 and CIRCUIT #2, shall be provided. Their functions are identical, except for the CPU Serial Communications Port and external connector (CIRCUIT #1 to SP1 [or SP3] and Connector C21S and CIRCUIT #2 to SP2 [or SP4] and Connector C22S).

7.3.2 Type 2070-7A

Each circuit shall convert its EIA-485 signal lines (RX, TX, RTS, CTS and DCD) to/from board TTL Level Signals; isolate both signal and ground; and drive / receive external EIA-232 devices via C21 / C22 Connectors. Connectors shall be DB-9S type.

7.3.3 Type 2070-7B

Each circuit EIA -485 signal lines, (RX, TX, TXC (I), TXC (O) and RXC) and associated signal ground shall be board terminated to matching drivers/receivers;

isolated both signal and ground, and drive/receiver external EIA-485 devices via C21/C22 Connectors. Connectors shall be DB-15S type.

7.3.4 Indicators

Each circuit signal TX and RX line shall have an LED Indicator mounted on the front plate and labeled to function.

SECTION 8 - TESTING

8.1 General

The equipment covered by this specification shall be subjected to following tests to determine conformance with all requirements of these specifications. The controller vendor shall arrange for and conduct all tests in accordance with the testing requirements stated herein.

The result of each test shall be compared with the requirements specified herein. Failure to conform to the requirements of any test shall be counted as a defect, and the equipment shall be subject to rejection. Rejected equipment may be offered again for a re-test, in accordance with Section A601 of the Department's current Minimum Specifications For Traffic Control Signal Devices (MSTCSD), provided that all areas in non-compliance have been corrected and re-tested by the controller vendor and evidence thereof submitted to the State Traffic Engineering Office.

8.2 Independent Environmental Lab Tests

The equipment shall meet all the environmental requirements outlined in Section A615 of the Department's MSTCSD. A test report certified by an independent laboratory shall be provided at the time of equipment submission.

8.3 National Transportation Communications for ITS Protocol (NTCIP) Requirement

All Model 2070 Controllers shall comply with the National Transportation Communications for ITS Protocol.

Software shall comply with NEMA Standards Publication TS 3.5 1996, NTCIP Object Definitions for Actuated Traffic Signal Controller Units, Version 96.01.7, April 1997.

(This requirement is not applicable until final development of the NTCIP standard is adopted unless specifically defined in system requirements. The controllers will be required to comply with the future Florida DOT ASC MIB which is currently under development.)

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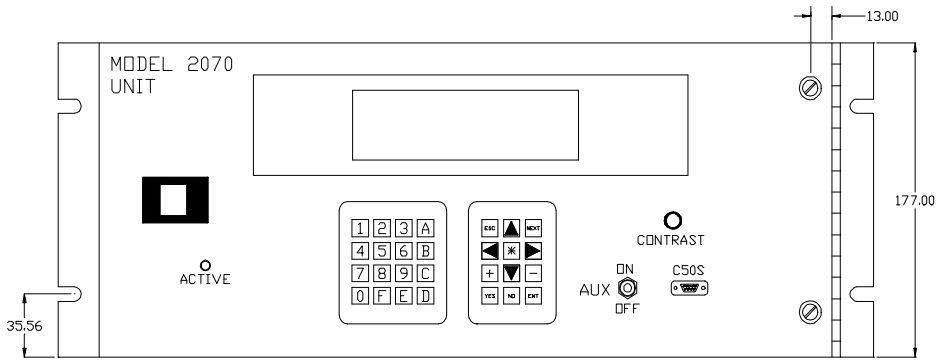
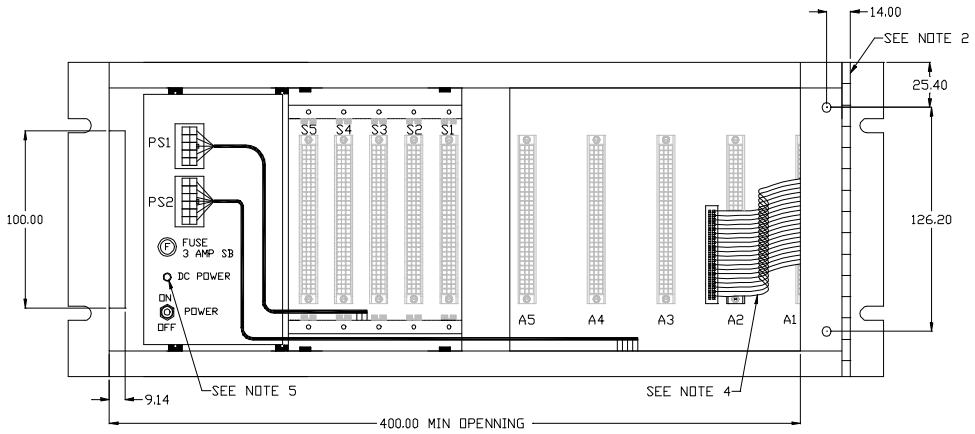
Type 2070-5	-	VME Cage Assembly	4-7-14
Type 2070-6	-	Async/Modem Serial Comm Module	5-5-1
Type 2070-7	-	Serial Comm Module	5-5-2

Notes:
All dimensions are in millimeters.



FRONT PANEL INSTALLED



FRONT PANEL REMOVED

NOTES (THIS DETAIL)

1. The unit shall be capable of mounting to a Standard EIA-310B Rack using 4U open end mounting slots.

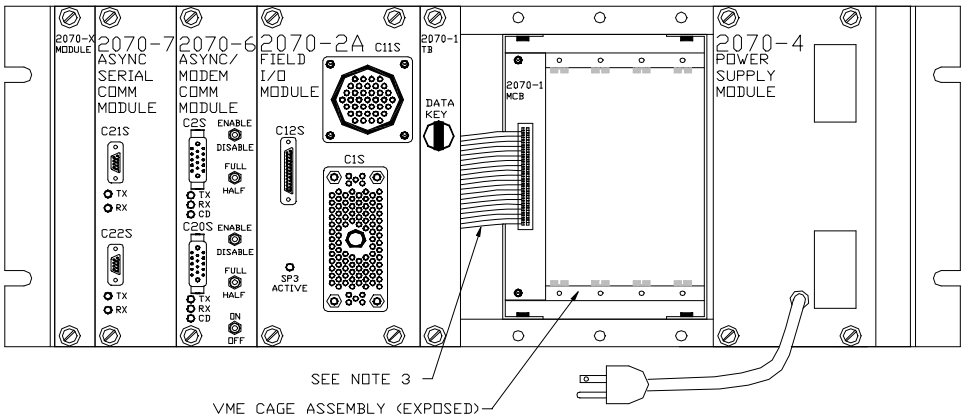
2. Continuous stainless steel hinge (4mm maximum hinge barrel) that attaches to the Front Panel by two TSD #1 Thumbscrew devices.

3. Actual location of ACTIVE light and contrast control shall be limited to ACTIVE light on the left side of the panel and the contrast control on the right side. They shall be located greater than 25.4 mm from other devices, connector or latch.

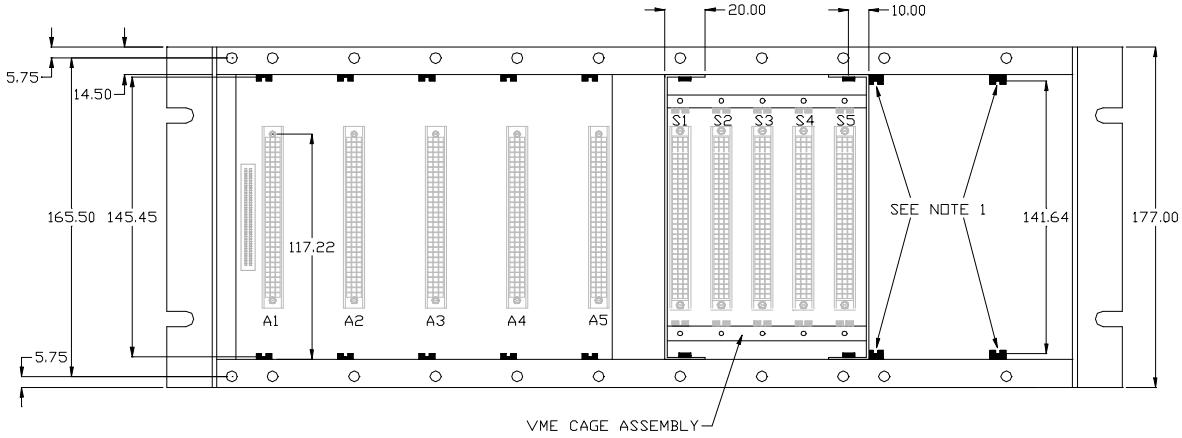
4. The length of the Front Panel Harness shall be no less than 284 mm.

5. A LED indicator for each DC voltage shall be provided.

	TITLE: MODEL 2070 CHASSIS FRONT VIEW	
	NO SCALE	
	TEES, NOV 19, 1998	9-7-1



REAR VIEW, LOADED



REAR VIEW, UNLOADED

NOTES (THIS DETAIL)

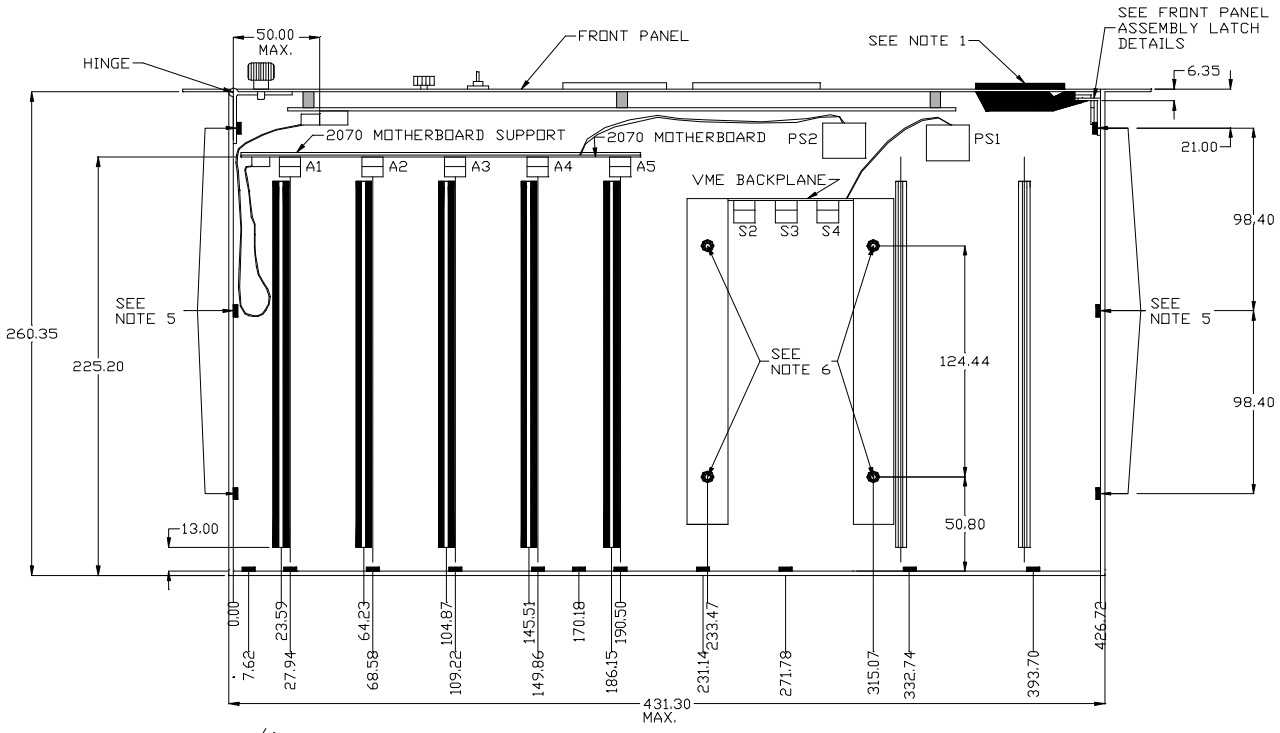
1. Four permanently attached 203.2 mm long Card Guides SAE 1800F (OR EQUAL) beginning 13 mm from the backplane mounting surface.

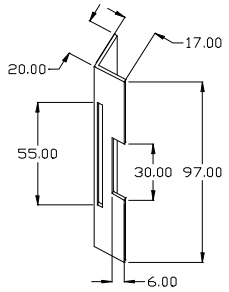
2. TB - TRANSITION BOARD
   MCB - MAIN CONTROLLER BOARD

3. Maximum length of harness shall be 101.60 mm, and shall not protrude beyond the back of the 2070 unit.

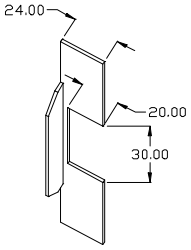
4. The VME Cage Assembly Openning shall be delivered covered by a blank panel. Matching M3 PEM fasteners shall be provided on the back plane surface for panel mounting.

	TYPE 2070 CHASSIS REAR VIEW	
	NO SCALE	
	NOV 19, 1998	4-7-2

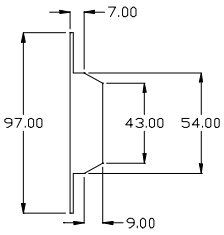




CHASSIS BRACKET



FRONT PANEL BRACKET



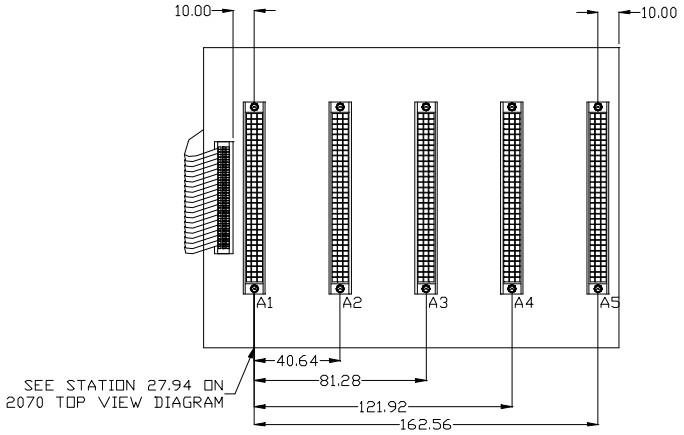
SIDE VIEW

FRONT PANEL ASSEMBLY LATCH DETAILS

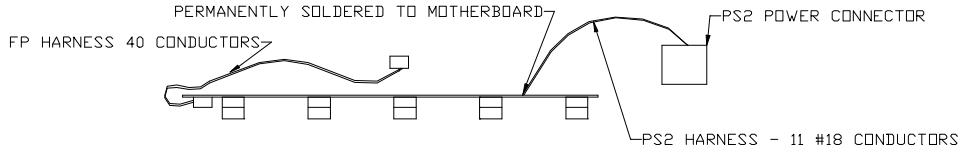
NOTES (THIS DETAIL)

1. Front Panel Assembly Latch mating with and rigidly held in place by Chassis Guide Latch/member shall be provided. The member shall vertically support the Front Panel Assembly in two other points besides the Latch.
2. Nylon card guides, SAE 1800F (OR EQUAL), shall be provided (top and bottom) for Mother Slot/Connectors A1 to A5. The Guides shall begin 13 mm from the Backplane surface.
3. M3 PEM Self-clinching Miniature Fasteners (OR EQUAL) shall be used for mounting holes located on Backplane Surface.
4. All harnesses shall have a minimum slack of 25 mm when connected.
5. M3 PEM Self-clinching Miniature Fasteners (OR EQUAL) shall be used for mounting holes to match the TSD #3 Thumbscrew Devices on the Type 2070-8 Module. Fastener centers shall be 6.35 mm above unit baseline.
6. Eight 6-32 Phillips head counter-sunk screws, 4 top and 4 bottom, shall be used to mount the cage assembly to the 2070 Chassis.
7. The 2070 chassis top & bottom sections shall be constructed with a continuous 15.77 mm folded lip along the front perpendicular to the 2070 top and bottom sections. The top and bottom sections of the 2070 chassis shall be recessed 18 mm as measured from the front surface of the front panel.

	TITLE: TYPE 2070 CHASSIS TOP VIEW	
	NO SCALE	
	NOV 19, 1998	4-7-3



FRONT VIEW



TOP VIEW

FP HARNESS PIN/WIRING ASSIGNMENT			
PIN	CONNECTOR ROW A	PIN	CONNECTOR ROW B
1	SP4-TXD+	2	SP4-TXD-
3	SP4-RXD+	4	SP4-RXD-
5	SP6-TXD+	6	SP6-TXD-
7	SP6-RXD+	8	SP6-RXD-
9	NA	10	NA
11	NA	12	NA
13	NA	14	NA
15	NA	16	NA
17	NA	18	NA
19	NA	20	NA
21	DC GROUND #1	22	DC GROUND #1
23	+12 VDC SERIAL	24	-12 VDC SERIAL
25	DC GROUND #1	26	DC GROUND #1
27	CPU LED	28	DC GROUND #1
29	CPURESET	30	DC GROUND #1
31	DC GROUND #1	32	NA
33	DC GROUND #1	34	+5 VDC
35	+5 VDC	36	+5 VDC
37	+5 VDC	38	+5 VDC
39	C50 ENABLE	40	C60 ENABLE

PS2 HARNESS PIN/WIRING ASSIGNMENT	
PIN	FUNCTION
1	+5 VDC
2	+12 VDC SERIAL
3	-12 VDC SERIAL
4	DC GND #1 (+5 VDC & 12 SERIAL)
5	+5 VDC STANDBY
6	+12 VDC - ISOLATED
7	DC GROUND #2 (+12 VDC ONLY)
8	POWER DOWN
9	POWER UP / SYS RESET
10	EQUIPMENT GROUND
11	LINESYNC
12	NA

NOTES (THIS DETAIL)

1. The Motherboard shall be a 3.175 mm minimum thickness pcb mechanically mounted in a vertical position.

2. A1 to A5 receptacle connectors shall be 96 socket contact DIN 41612 connectors (ROBINSON NUGENT #DIN 96RSC or ELCO Series 8477 Three Row Inverted Socket OR EQUAL).

3. The location of the FP Harness on either side of the motherboard is allowed. The FP Harness shall either be directly soldered to the motherboard or a header used.

TITLE: TYPE 2070 CHASSIS MOTHERBOARD

NO SCALE

NOV 19, 1998 | 4-7-4

A1 CONNECTOR PIN OUT			
PIN	A	B	C
1	SP3TXD+	SP6TXD+	SP5TXD+
2	SP3TXD-	SP6TXD-	SP5TXD-
3	SP3RXD+	SP6RXD+	SP5TXC+
4	SP3RXD-	SP6RXD-	SP5TXC-
5	SP3RTS+	SP3TXCO+	SP5RXD+
6	SP3RTS-	SP3TXCO-	SP5RXD-
7	SP3CTS+	SP3TXCI+	SP5RXC+
8	SP3CTS-	SP3TXCI-	SP5RXC-
9	SP3DCD+	SP3RXC+	SP3TXD+
10	SP3DCD-	SP3RXC-	SP3TXD-
11	SP4TXD+	SP4TXD+	SP3RXD+
12	SP4TXD-	SP4TXD-	SP3RXD-
13	SP4RXD+	SP4RXD+	SP3RTS+
14	SP4RXD-	SP4RXD-	SP3RTS-
15	NA	NA	SP3CTS+
16	NA	NA	SP3CTS-
17	NA	NA	SP3DCD+
18	NA	NA	SP3DCD-
19	NA	NA	SP3TXCO+
20	NA	NA	SP3TXCO-
21	DCG #1	C50 ENABLE	SP3TXCI+
22	NETWK1	NA	SP3TXCI-
23	NETWK2	NA	SP3RXC+
24	DCG #1	LINESYNC	SP3RXC-
25	NETWK3	POWERUP	CPURESET
26	NETWK4	POWERDN	FPLED
27	DCG #1	DCG #1	DCG #1
28	+12 SER	-12 SER	+5 STDBY
29	+5 VDC	+5 VDC	+5 VDC
30	DCG #1	DCG #1	DCG #1
31	+12 VDC	+12 VDC	+12 VDC
32	DCG #2	DCG #2	DCG #2

A2 TO A5 CONNECTOR PIN OUT			
PIN	A	B	C
1	SP1TXD+	SP6TXD+	SP5TXD+
2	SP1TXD-	SP6TXD-	SP5TXD-
3	SP1RXD+	SP6RXD+	SP5TXC+
4	SP1RXD-	SP6RXD-	SP5TXC-
5	SP1RTS+	SP1TXC0+	SP5RXD+
6	SP1RTS-	SP1TXC0-	SP5RXD-
7	SP1CTS+	SP1TXCI+	SP5RXC+
8	SP1CTS-	SP1TXCI-	SP5RXC-
9	SP1DCD+	SP1RXC+	SP3TXD+
10	SP1DCD-	SP1RXC-	SP3TXD-
11	SP2TXD+	SP4TXD+	SP3RXD+
12	SP2TXD-	SP4TXD-	SP3RXD-
13	SP2RXD+	SP4RXD+	SP3RTS+
14	SP2RXD-	SP4RXD-	SP3RTS-
15	SP2RTS+	SP2TXCO+	SP3CTS+
16	SP2RTS-	SP2TXCO-	SP3CTS-
17	SP2CTS+	SP2TXCI+	SP3DCD+
18	SP2CTS-	SP2TXCI-	SP3DCD-
19	SP2DCD+	SP2RXC+	SP3TXCO+
20	SP2DCD-	SP2RXC-	SP3TXCO-
21	DCG #1	(SEE NOTE 4)	SP3TXCI+
22	NETWK1	(SEE NOTE 4)	SP3TXCI-
23	NETWK2	(SEE NOTE 4)	SP3RXC+
24	DCG #1	LINESYNC	SP3RXC-
25	NETWK3	POWERUP	CPURESET
26	NETWK4	POWERDN	FPLED
27	DCG #1	DCG #1	DCG #1
28	+12 SER	-12 SER	+5 STDBY
29	+5 VDC	+5 VDC	+5 VDC
30	DCG #1	DCG #1	DCG #1
31	+12 VDC	+12 VDC	+12 VDC
32	DCG #2	DCG #2	DCG #2

NOTES (THIS DETAIL)

1. Functions are referenced to the CPU.
2. DC GND #1 for +5VDC and +12VDC Serial.
   DC GND #2 for +12VDC ISO.
3. A1 Connector is furthest A Connector to the left when viewed from the unit back. All A Connectors are pin assigned the same.
4. Connector A2 to A4, pins B21 and B22 shall read "NA".

   Connector A2, pin B23 shall read "A2 Installed".

   Connector A3, pin B23 shall read "A3 Installed".

   Connector A5, pin B21 shall read "A2 Installed".

   Connector A5, pin B22 shall read "DCG #1".

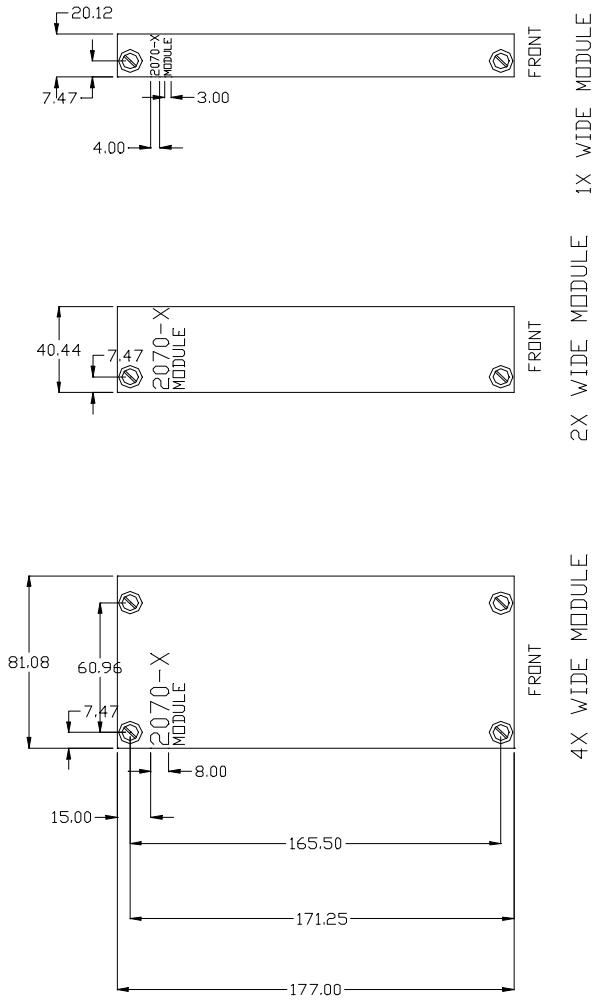
   Connector A5, pin B23 shall read "A3 Installed".

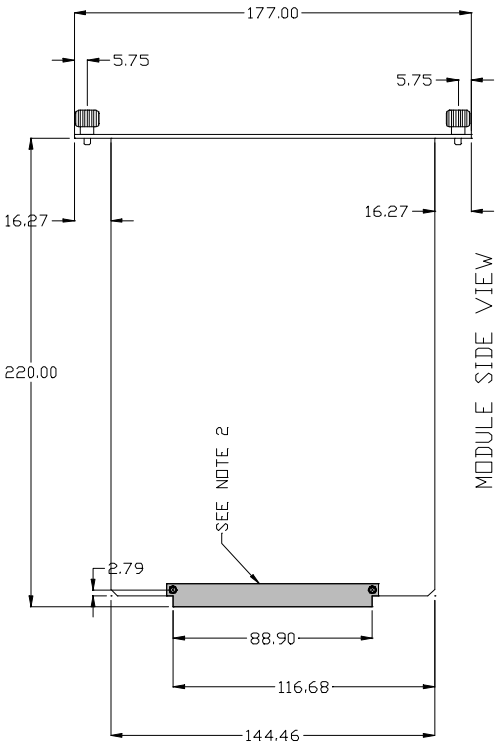
TITLE: Motherboard A Connector Pin Assignment

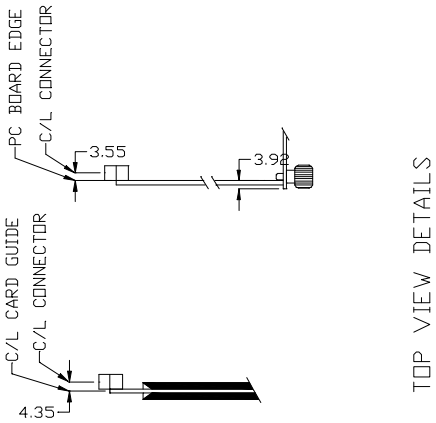
NO SCALE

TEES, NOV 19, 1998

9-7-5







NOTES (THIS DETAIL)

1. All Thumbscrew devices on modules described in this drawing shall be TD#3 OR EQUAL.

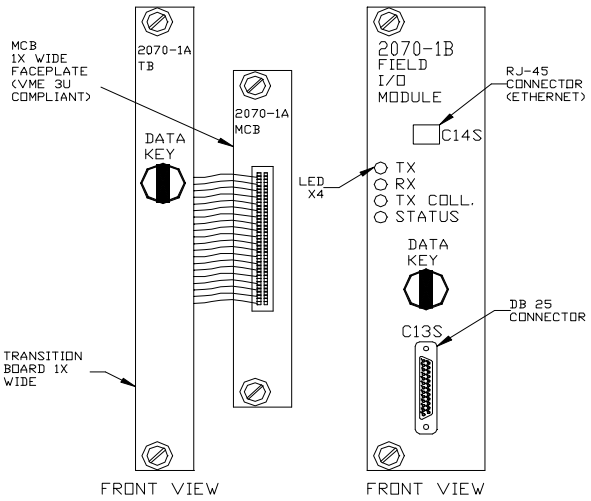
2. 96 pin DIN connector ELCO # 00 8272 96 000 013 OR EQUAL.

	TITLE: TYPE 2070 SYSTEM PCB MODULES, GENERAL	
	NO SCALE	
	NOV 19, 1998	4-7-6

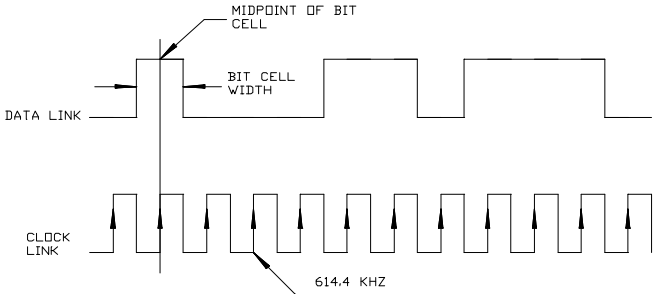
SERIAL PORT REQUIREMENTS

A2 TO A5 CONNECTOR PIN OUT			
LOGICAL PORT	68360 PORT	RATE KBITS	PROTOCOL
SP1	SEE NOTE 4	(1)	ASYNC
SP1S	SEE NOTE 4	(2)	SYNC, HDLC, SDLC
SP2	SCC2	(1)	ASYNC
SP2S	SCC2	(2)	SYNC, HDLC, SDLC
SP3	SCC4	(1)	ASYNC
SP3S	SCC4	153.6, 614.4*	SYNC, HDLC, SDLC
SP4	SMC2	(1)	ASYNC
SP5	SCC3	(1)	ASYNC
SP5S	SCC3	153.6, 614.4*	SYNC, HDLC, SDLC
SP6	SMC1	(1), 38.4*	ASYNC

SDLC FRAME LAYOUT					
OPENNING FLAG	ADDR	CONTROL	INFORMATION	CRC	CLOSING FLAG
0111 1110	8 BITS	1000 0011	VARIABLE LENGTH	16 BITS	0111 1110



CPU FACE PANELS



SDLC TIMING

C13S PIN ASSIGNMENT			
PIN	FUNCTION	PIN	FUNCTION
1	SP8 TX +	14	SP8 TX -
2	SP8 RX +	15	SP8 RX -
3	SP8 TXC +	16	SP8 TXC -
4	SP8 RXC +	17	SP8 RXC -
5	SP8 RTS + **	18	SP8 RTS - **
6	SP8 CTS + **	19	SP8 CTS - **
7	SP8 DCD + **	20	SP8 DCD - **
8	NA	21	NA
9	LINESYNC +	22	LINESYNC -
10	NRESET +	23	NRESET -
11	PWRDWN +	24	PWRDWN -
12	+5 VDC	25	EQUIP GND
13	DC GND #2		

NOTES (THIS DETAIL)

1. (1) BPS Rates 1.2* 2.4, 4.8, 9.6, 19.2, 38.4

2. (2) BPS Rates 19.2*, 38.4, 57.6, 76.8, 153.6

3. * Default BPS Rate for indicated Port.
   ** Disconnected by internal switch.

4. SP1 OF THE 2070-1A is 68360 SCC1. SP1 OF THE 2070-1B is Dual SCC1 with 68360 SCC1 assigned to ETHERNET.

5. A Post Header (ROBINSON NUGENT IDA-XX OR EQUAL) Connector with strain relief shall be provided on the MCB Front Plate and the Transition Board for mating with the interface harness. The harness shall be shielded and straight through wired.

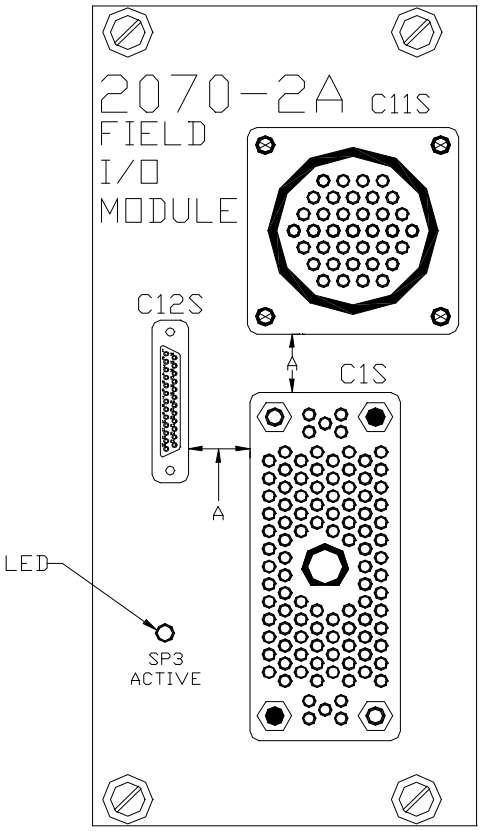
C14S PIN ASSIGNMENT (ETHERNET)			
PIN	FUNCTION	PIN	FUNCTION
1	TX +	5	NA
2	TX -	6	RX -
3	RX +	7	NA
4	NA	8	NA

TITLE: TYPE 2070-1 CPU MODULES AND SERIAL PORT/SDLC PROTOCOL

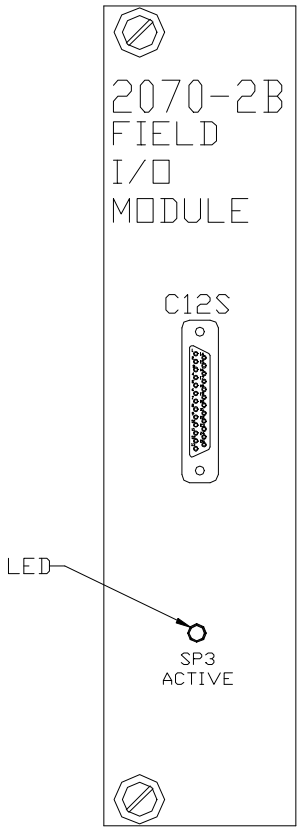
NO SCALE

NOV 19, 1998

4-7-7



FRONT VIEW



FRONT VIEW

FIELD I/O FACE PANELS

NOTES (THIS DETAIL)

1. 2070-2A Faceplate shall be 4X wide.
   2070-2B Faceplate shall be 2X wide.
   (SEE SYSTEM PCB MODULE, GENERAL DETAILS.)

2. Dark Circles in the C1S Connector denote guide pin locations and open circles denote guide socket locations.

3. Dimension "A" shall be a minimum of 12.7 mm.

4. C1S - M104 Type
   C11S - 37-Pin Circular Plastic Type
   C12S - 25-Pin DB Socket Type

C12S PIN ASSIGNMENT

PIN	FUNCTION	PIN	FUNCTION
1	TX5 DATA +	14	TX5 DATA -
2	RX5 DATA +	15	RX5 DATA -
3	TX5 CLOCK +	16	TX5 CLOCK -
4	RX5 CLOCK +	17	RX5 CLOCK -
5	TX3 DATA +	18	TX3 DATA -
6	RX3 DATA +	19	RX3 DATA -
7	TX3 CLOCK +	20	TX3 CLOCK -
8	RX3 CLOCK +	21	RX3 CLOCK -
9	LINE SYNC +	22	LINE SYNC -
10	NRESET +	23	NRESET -
11	POWER DOWN +	24	POWER DOWN -
12	+5 VDC	25	EQUIP GND
13	DC GND #2		

TITLE:

TYPE 2070-2
FIELD I/O MODULES

NO SCALE

NOV 19, 1998

4-7-8

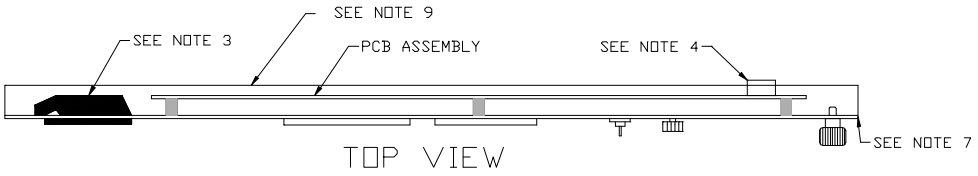
C1S PIN ASSIGNMENT

PIN	FUNCTION NAME	FUNCTION PORT	PIN	FUNCTION NAME	FUNCTION PORT	PIN	FUNCTION NAME	FUNCTION PORT	PIN	FUNCTION NAME	FUNCTION PORT
1	DC GROUND		27	O24	O4-1	53	I14	I2-7	79	I44	I6-5
2	O0	O1-1	28	O25	O4-2	54	I15	I2-8	80	I45	I6-6
3	O1	O1-2	29	O26	O4-3	55	I16	I3-1	81	I46	I6-7
4	O2	O1-3	30	O27	O4-4	56	I17	I3-2	82	I47	I6-8
5	O3	O1-4	31	O28	O4-5	57	I18	I3-3	83	O40	O6-1
6	O4	O1-5	32	O29	O4-6	58	I19	I3-4	84	O41	O6-2
7	O5	O1-6	33	O30	O4-7	59	I20	I3-5	85	O42	O6-3
8	O6	O1-7	34	O31	O4-8	60	I21	I3-6	86	O43	O6-4
9	O7	O1-8	35	O32	O5-1	61	I22	I3-7	87	O44	O6-5
10	O8	O2-1	36	O33	O5-2	62	I23	I3-8	88	O45	O6-6
11	O9	O2-2	37	O34	O5-3	63	I28	I4-5	89	O46	O6-7
12	O10	O2-3	38	O35	O5-4	64	I29	I4-6	90	O47	O6-8
13	O11	O2-4	39	I0	I1-1	65	I30	I4-7	91	O48	O7-1
14	DC GROUND		40	I1	I1-2	66	I31	I4-8	92	DC GROUND	
15	O12	O2-5	41	I2	I1-3	67	I32	I5-1	93	O49	O7-2
16	O13	O2-6	42	I3	I1-4	68	I33	I5-2	94	O50	O7-3
17	O14	O2-7	43	I4	I1-5	69	I34	I5-3	95	O51	O7-4
18	O15	O2-8	44	I5	I1-6	70	I35	I5-4	96	O52	O7-5
19	O16	O3-1	45	I6	I1-7	71	I36	I5-5	97	O53	O7-6
20	O17	O3-2	46	I7	I1-8	72	I37	I5-6	98	O54	O7-7
21	O18	O3-3	47	I8	I2-1	73	I38	I5-7	99	O55	O7-8
22	O19	O3-4	48	I9	I2-2	74	I39	I5-8	100	O36	O5-5
23	O20	O3-5	49	I10	I2-3	75	I40	I6-1	101	O37	O5-6
24	O21	O3-6	50	I11	I2-4	76	I41	I6-2	102	O38 DET RES	O5-7
25	O22	O3-7	51	I12	I2-5	77	I42	I6-3	103	O39 WDT	O5-8
26	O23	O3-8	52	I13	I2-6	78	I43	I6-4	104	DC GROUND	

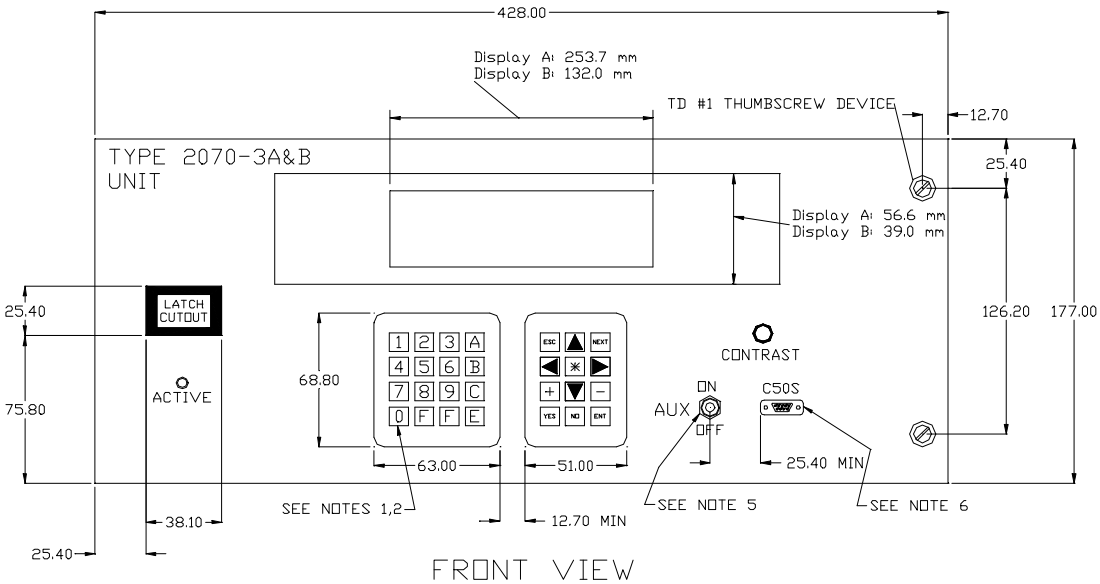
C11S PIN ASSIGNMENT

PIN	FUNCTION NAME	FUNCTION PORT	PIN	FUNCTION NAME	FUNCTION PORT	PIN	FUNCTION NAME	FUNCTION PORT	PIN	FUNCTION NAME	FUNCTION PORT
1	O56	O8-1	11	I25	I4-2	21	I54	I7-7	31	DC GROUND	
2	O57	O8-2	12	I26	I4-3	22	I55	I7-8	32	NA	- - -
3	O58	O8-3	13	I27	I4-4	23	I56	I8-1	33	NA	- - -
4	O59	O8-4	14	DC GROUND		24	I57	I8-2	34	NA	- - -
5	O60	O8-5	15	I48	I7-1	25	I58	I8-3	35	NA	- - -
6	O61	O8-6	16	I49	I7-2	26	I59	I8-4	36	NA	- - -
7	O62	O8-7	17	I50	I7-3	27	I60	I8-5	37	DC GROUND	
8	O63	O8-8	18	I51	I7-4	28	I61	I8-6			
9	DC GROUND		19	I52	I7-5	29	I62	I8-7			
10	I24	I4-1	20	I53	I7-6	30	I63	I8-8			

TITLE:	TYPE 2070-2A FIELD I/O MODULE C1 & C11 CONNECTORS
NO SCALE	
NOV 19, 1998	4-7-9



TOP VIEW



FRONT VIEW

NOTES (THIS DETAIL)

1. Key size shall be 7.62 X 7.62.
2. Key center to center spacing shall be 12.70 mm.
3. Slide latch shall be a SOUTHCO flush style A3-40-625-12 (OR EQUAL).
4. 40 contact FP harness pin header connector. It shall be compatible to the FP harness in type and pin assignments. The center of the FP Harness Pin Header shall be vertically positioned between 85 and 95 mm as measured from the top of the FPA.
5. Two position CONTROL switch mounted vertically.
6. "C50S" connector shall be a DB-9 socket contact connector.
7. Fron panel sheet metal thickness shall be 1.52 ±0.13.
8. All FPA devices shall be located as shown.
9. The FPA shall be provided with a continuous top and bottom 17 mm lip bent 90 degrees to the front plate and shall extend the full length of the FPA.

C50S CONNECTOR PINOUTS	
PIN	C50S FUNCTION
1	C50 - ENABLE
2	SP4 RX
3	SP4 TX
4	NA
5	DC GROUND #1
6	NA
7	NA
8	NA
9	NA

C60S CONNECTOR PINOUTS	
PIN	FUNCTION
1	NA
2	SP6 RX
3	SP6 TX
4	NA
5	DC GROUND #1
6	NA
7	CPU RESET
8	NA
9	CPU LED

TYPE 2070-3A&B
FRONT PANEL ASSEMBLY

NOV 19, 1998 | 4-7-10

TYPE 2070-3 AUX SWITCH CODES		
SWITCH POSITION	ASCII DATA (TEXT)	ASCII DATA (HEX)
ON	ESC O T	1B 4F 54
OFF	ESC O U	1B 4F 55

TYPE 2070-3 KEY CODES		
KEY	ASCII DATA (TEXT)	ASCII DATA (HEX)
0	0	30
1	1	31
2	2	32
3	3	33
4	4	34
5	5	35
6	6	36
7	7	37
8	8	38
9	9	39
A	A	41
B	B	42
C	C	43
D	D	44
E	E	45
F	F	46
(UP ARROW)	ESC [A	1B 5B 41
(DOWN ARROW)	ESC [B	1B 5B 42
(RIGHT ARROW)	ESC [C	1B 5B 43
(LEFT ARROW)	ESC [D	1B 5B 44
ESC	ESC O S	1B 4F 53
NEXT	ESC O P	1B 4F 50
YES	ESC O Q	1B 4F 51
NO	ESC O R	1B 4F 52
*	*	2A
+	+	2B
-	-	2D
ENTER	CR	0D

	TITLE: TYPE 2070-3 FRONT PANEL ASSEMBLY KEY CODES	
	NO SCALE	
	NOV 19, 1998	4-7-11

CONFIGURATION COMMAND CODES

ASCII REPRESENTATION	HEX VALUE	FUNCTION
HT	09	Move cursor to next tab stop
CR	0D	Position cursor at first position on current line
LF	0A	(Line Feed) Move cursor down one line
BS	08	(Backspace) Move cursor one position to the left and write space
ESC [Py ; Px f	1B 5B Py 3B Px 66	Position cursor at (Px, Py)
ESC [Pn C	1B 5B Pn 43	Position cursor Pn positions to right
ESC [Pn D	1B 5B Pn 44	Position cursor Pn positions to left
ESC [Pn A	1B 5B Pn 41	Position cursor Pn positions up
ESC [Pn B	1B 5B Pn 42	Position cursor Pn positions down
ESC [H	1B 5B 48	Home cursor (move to 1,1)
ESC [2 J	1B 5B 32 4A	Clear screen with spaces without moving cursor
ESC c	1B 63	Soft reset
ESC P P1 [Pn ; Pn...f	1B 50 P1 5B Pn 3B...Pn 66	Compose special character number Pn (1-8) at current cursor position
ESC [< Pn V	1B 5B 3C Pn 56	Display special character number Pn (1-8) at current cursor position
ESC [25 h	1B 5B 32 35 68	Turn Character blink on
ESC [25 l	1B 5B 32 35 6C	Turn character blink off
ESC [< 5 h	1B 5B 3C 35 68	Illuminate Backlight
ESC [< 5 l	1B 3B 3C 35 6C	Extinguish Backlight
ESC [33 h	1B 5B 33 33 68	Cursor blink on
ESC [33 l	1B 5B 33 33 6C	Cursor blink off
ESC [27 h	1B 5B 32 37 68	Reverse video on
ESC [27 l	1B 5B 32 37 6C	Reverse video off
ESC [24 h	1B 5B 32 34 68	Underline on
ESC [24 l	1B 5B 32 34 6C	Underline off
ESC [0 m	1B 5B 30 6D	All attributes off
ESC H	1B 48	Set tab stop at current cursor position
ESC [Pn g	1B 5B Pn 67	Clear tab stop Pn = 0,1,2 at cursor = 3 all tab stops
ESC [? 7 h	1B 5B 3F 37 68	Auto-wrap on
ESC [? 7 l	1B 5B 3F 37 6C	Auto-wrap off
ESC [? 8 h	1B 5B 3F 38 68	Auto-repeat on
ESC [? 8 l	1B 5B 3F 38 6C	Auto-repeat off
ESC [? 25 h	1B 5B 3F 32 35 68	Cursor on
ESC [? 25 l	1B 5B 3F 32 35 6C	Cursor off
ESC [< 47 h	1B 5B 3C 34 37 68	Auto-scroll on
ESC [< 47 l	1B 5B 3C 34 37 6C	Auto-scroll off
ESC [< Pn S	1B 5B 3C Pn 53	Set Backlight timeout value to Pn (0-63)
ESC [PU	1B 5B 50 55	String sent to CPU when FPA power up.

NOTE: Numerical values have one ASCII character per digit without leading zero.

INQUIRY COMMAND-RESPONSE CODES

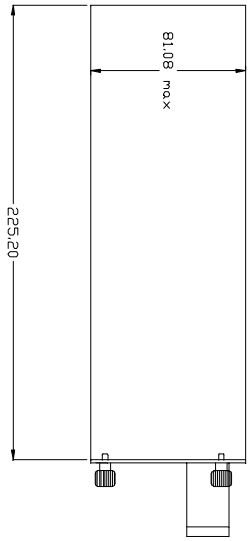
COMMAND CPU Module to Front Panel Module		RESPONSE Front Panel Module to CPU Module		FUNCTION
ASCII Representation	HEX Value	ASCII Representation	HEX Value	
ESC [6 n	1B 5B 36 6E	ESC [Py; Px R	1B 5B Py 3B Px 52	Inquire Cursor Position
ESC [B n	1B 5B 42 6E	ESC [P1;P2;....P6 R	1B 5B P1 3B P2 3B....P6 52	Status Cursor Position P1: Auto-wrap (h,l) P2: Auto-scroll (h,l) P3: Auto-repeat (h,l) P4: Backlight (h,l) P5: Backlight timeout P6: AUX Switch (h,l)
ESC [A n	1B 5B 41 6E	ESC [P1 R	1B 5B P1 52	P1: AUX Switch (h,l)

TITLE: TYPE 2070-3
FRONT PANEL ASSEMBLY
KEY CODES

NO SCALE

NOV 19, 1998

4-7-12



TOP VIEW

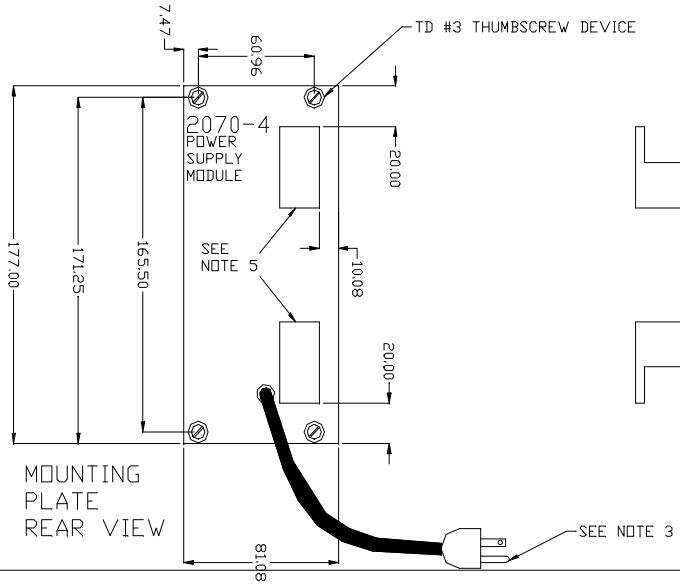
PS1 CONNECTOR PINOUT	
PIN	FUNCTION
1	+5 VDC
2	+12 VDC SERIAL
3	-12 VDC SERIAL
4	DC GND #1 (+5 VDC & 12 SERIAL)
5	+5 VDC STANDBY
6	+5 VDC SENSE
7	DC GROUND SENSE
8	AC FAIL (VME)
9	SYSRESET (VME)
10	NA

PS2 CONNECTOR PINOUT	
PIN	FUNCTION
1	+5 VDC
2	+12 VDC SERIAL
3	-12 VDC SERIAL
4	DC GND #1 (+5 VDC & 12 SERIAL)
5	+5 VDC STANDBY
6	+12 VDC
7	DC GROUND (+12 VDC ONLY)
8	POWER DOWN / AC FAIL
9	POWER UP / SYS RESET
10	EQUIPMENT GROUND
11	LINESYNC
12	NA

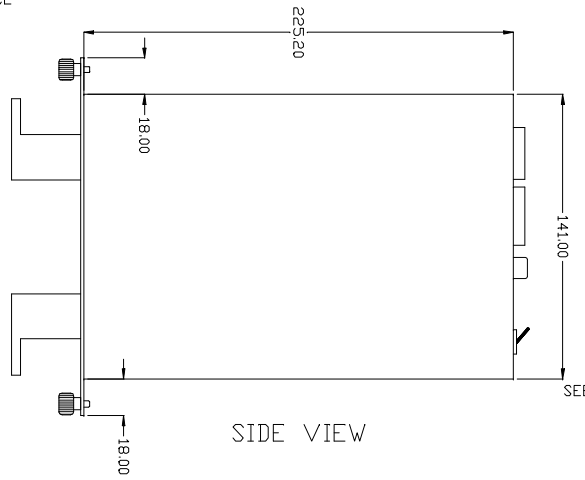
NOTES (THIS DETAIL)

1. Power switch shall be mounted vertically. Power On shall be in the up position.
2. Fuse shall be a replaceable 3AG Slow Blow type resident in a fuse holder. Fuse label shall indicate rating.
3. Three #16 conductor power cable, 1 meter minimum length and permanenlty attached to the Module with strain relief. The end plug connector shall be a three blade NEMA 5-15P grounding plug type.
4. PS1 and PSS2 Receptacle Connectors shall be AMP Mini-Universal Double row MATE-N-LOK CAP Connectors with locking latch devices (OR EQUAL).

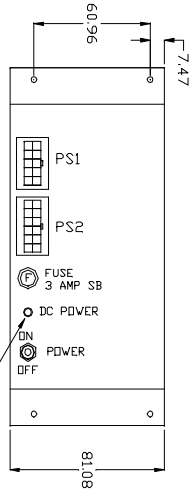
   PS1 connector shall be a 10 position PLUG connector. PS2 connector shall be a 12 position PLUG connector.
5. Buckeye Cord-Wrap PP-40055 device with PP-40058 Extension (OR EQUAL).
6. Mounting Plate shall conform to the 4X Wide Module dimensions.
7. A LED indicator shall be provided for each DC power source (+5, +12 ISO, +12 SER, and -12 SER).



MOUNTING
PLATE
REAR VIEW



SIDE VIEW



FRONT VIEW

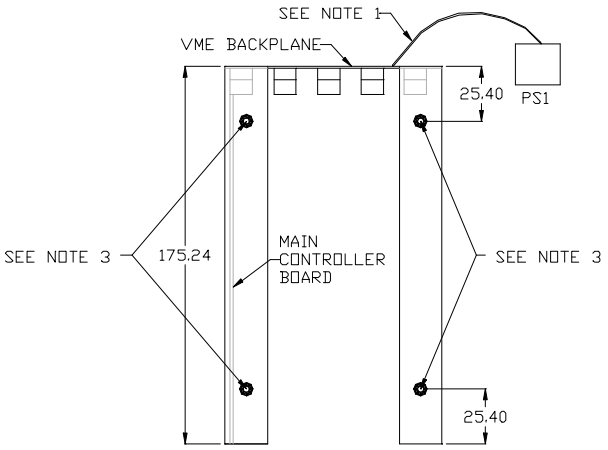
TITLE:

TYPE 2070-4
POWER SUPPLY MODULE

NO SCALE

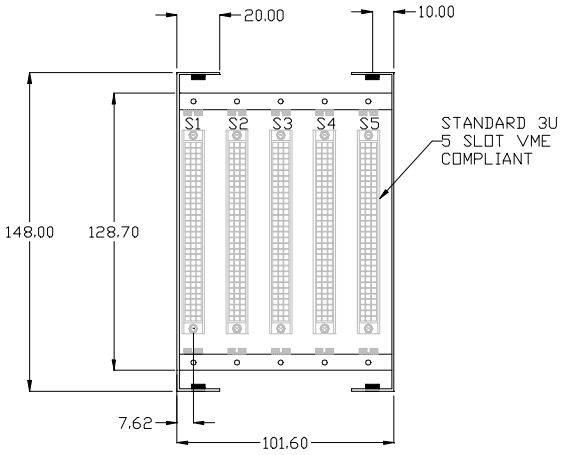
NOV 19, 1998

4-7-13



TOP VIEW

PS1 CONNECTOR PIN ASSIGNMENT	
PIN	FUNCTION
1	+5 VDC
2	+12 VDC SERIAL
3	-12 VDC SERIAL
4	DC GND #1 (+5 VDC & 12 SERIAL)
5	+5 VDC STANDBY
6	+5 VDC SENSE
7	DC GROUND SENSE
8	AC FAIL (VME)
9	SYSRESET (VME)
10	NA



FRONT VIEW

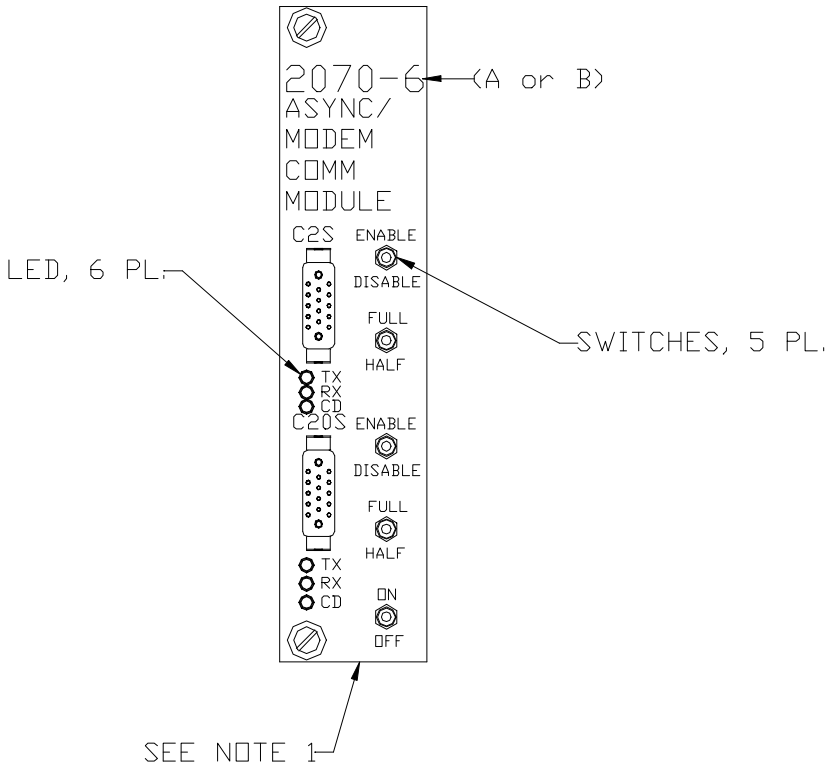
NOTES (THIS DETAIL)

1. PS1 Harness interfaces between the Type 2070-4 Power Supply Module and the 2070-5 VME Cage Assembly. The harness shall be permanently attached to the Cage Assembly by solder, FASTON or Power Bugs. The Harness wiring shall be 8 #18 conductors for power and 2 #22 conductors for others.

2. The Cage shall be mounted to a front mounting plate. The plate shall cover the open area and attach to the Chassis Backplane mounting surface via screws meeting the Chapter 1 external screw requirements. The screws shall mate with the PEM nuts as specified in the Type 2070 Chassis Top View Detail.

3. M3 PEM Self-clinching Miniature Fasteners (OR EQUAL) shall be used for mounting holes to match the 6-32 Phillips countersunk screws on the top and bottom of the Type 2070 chassis.

	TITLE: TYPE 2070-5 VME CAGE ASSEMBLY	
	NO SCALE	
	NOV 19, 1998	4-7-14



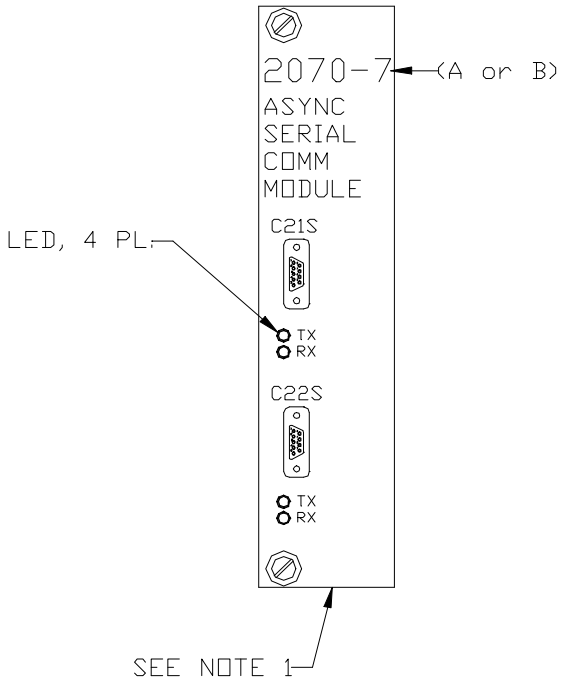
C2 & C20 CONNECTOR PINOUT			
PIN	FUNCTION	PIN	FUNCTION
A	AUDIO IN	J	RTS
B	AUDIO IN	K	DATA IN
C	AUDIO OUT	L	DATA OUT
D	ISO +5 VDC	M	CTS
E	AUDIO OUT	N	ISO DC GND
F	NA	P	NA
H	CD	R	NA

NOTES (THIS DETAIL)

1. 2X Faceplate (See System PCB Module, General Details).

2. Connectors C2S & C20S shall be mounted on the front plate and shall be M14 AMP with Spring Latch supports or equal.

	TITLE: TYPE 2070-6A, 6B ASYNC/MODEM SERIAL COMM MODULE	
	NO SCALE	
	NOV 19, 1998	5-5-1



2070-7A (DB-9S)	
C21 & C22 CONNECTOR PINOUT	
PIN	FUNCTION
1	DCD
2	RXD
3	TXD
4	NA
5	ISO DC GND
6	NA
7	RTS
8	CTS
9	NA

2070-7B (DB-15S)			
C21 & C22 CONNECTOR PINOUT			
PIN	FUNCTION	PIN	FUNCTION
1	TX DATA +	9	TX DATA -
2	ISO DC GND	10	ISO DC GND
3	TX CLOCK +	11	TX CLOCK -
4	ISO DC GND	12	ISO DC GND
5	RX DATA +	13	RX DATA -
6	ISO DC GND	14	ISO DC GND
7	RX CLOCK +	15	RX CLOCK -
8	NA		

NOTES (THIS DETAIL)

1. 2X Faceplate (See System PCB Module, General Details).

TITLE:
TYPE 2070-7A, 7B
SERIAL COMM MODULE

NO SCALE

NOV 19, 1998

5-5-2